

Project Name :GK5CN5Z

Platform : CFL-H+N17P-GX

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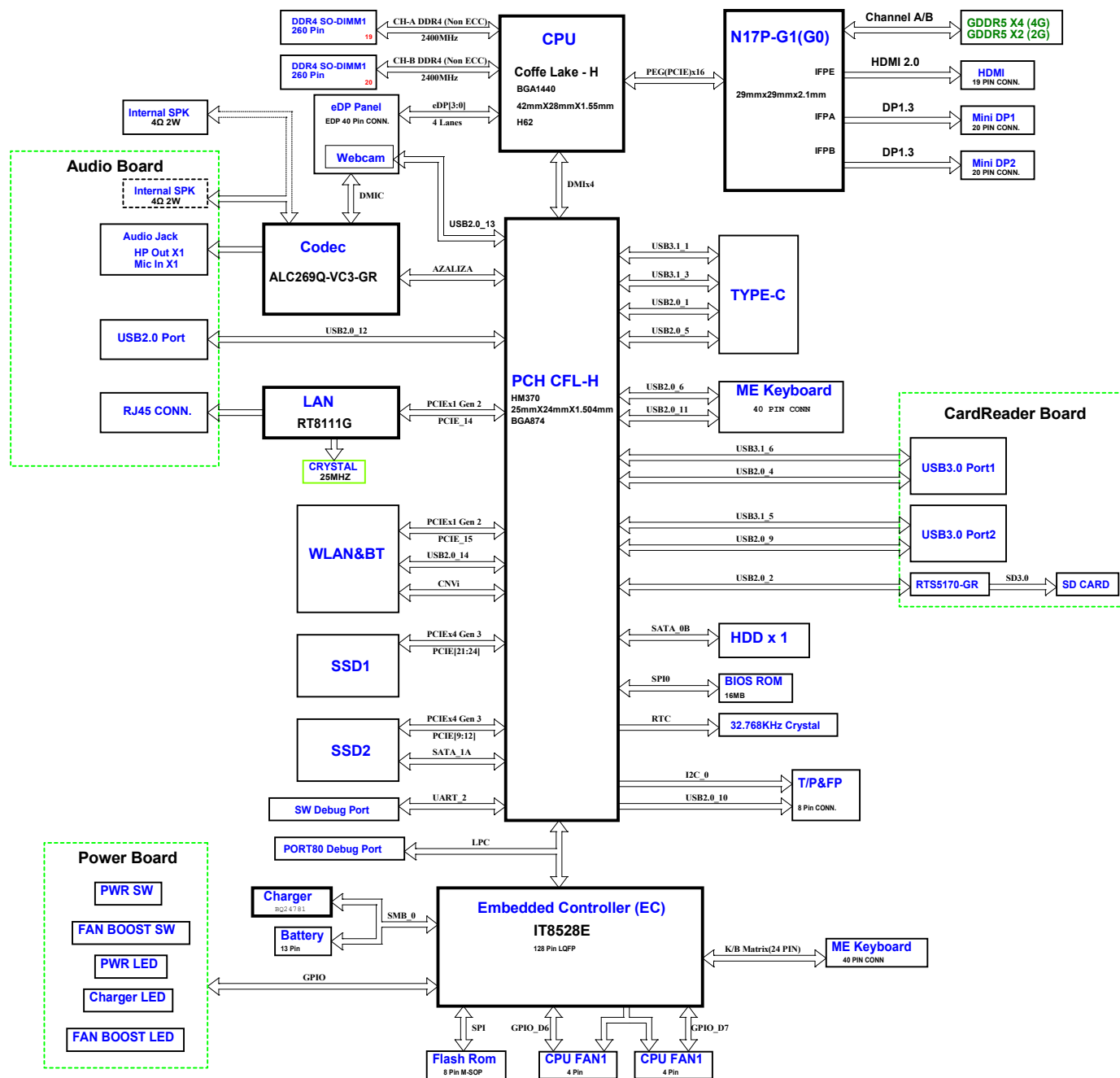
M/B Schematic Version Change List

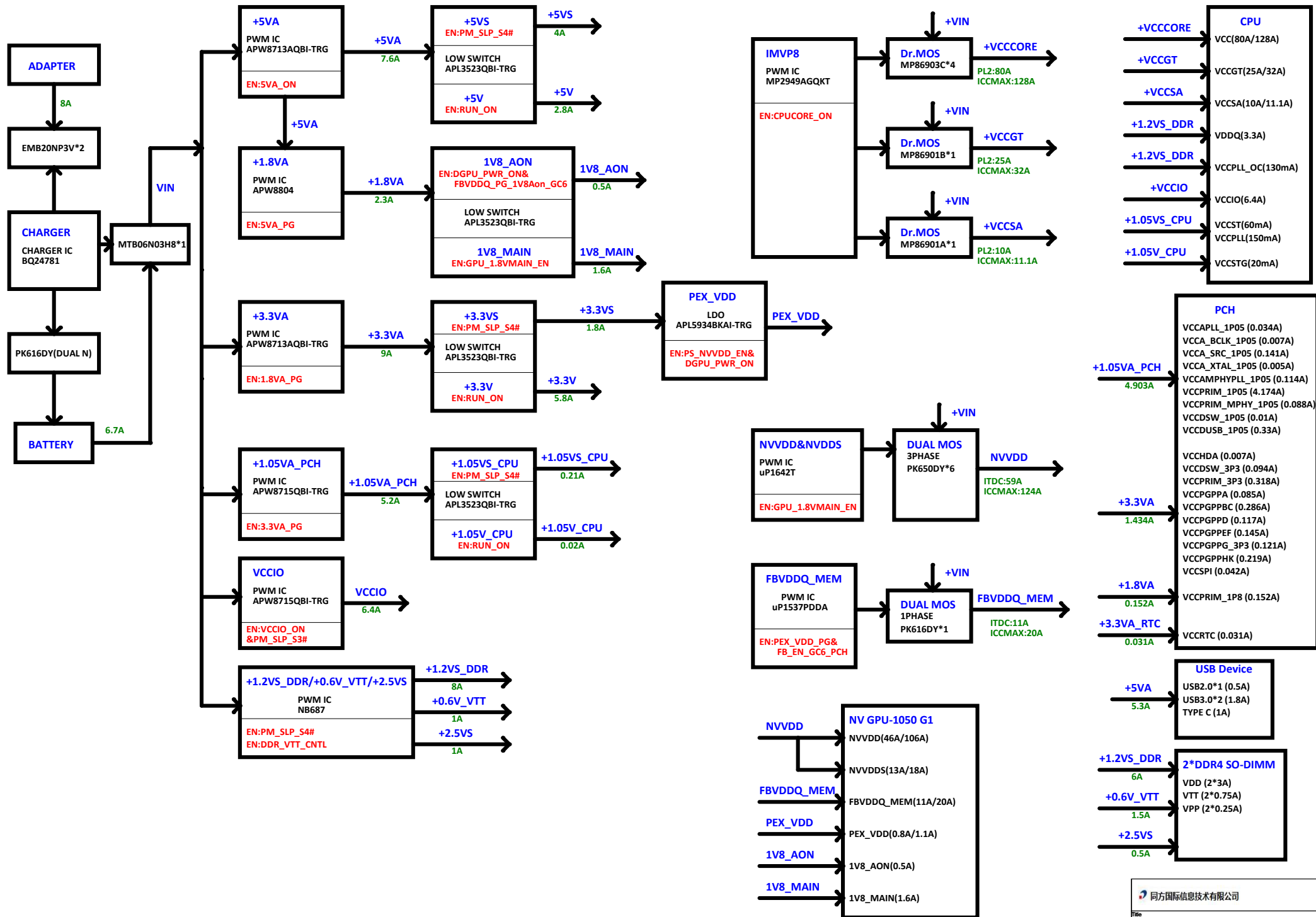
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

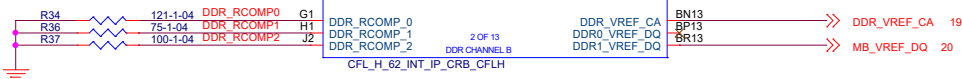
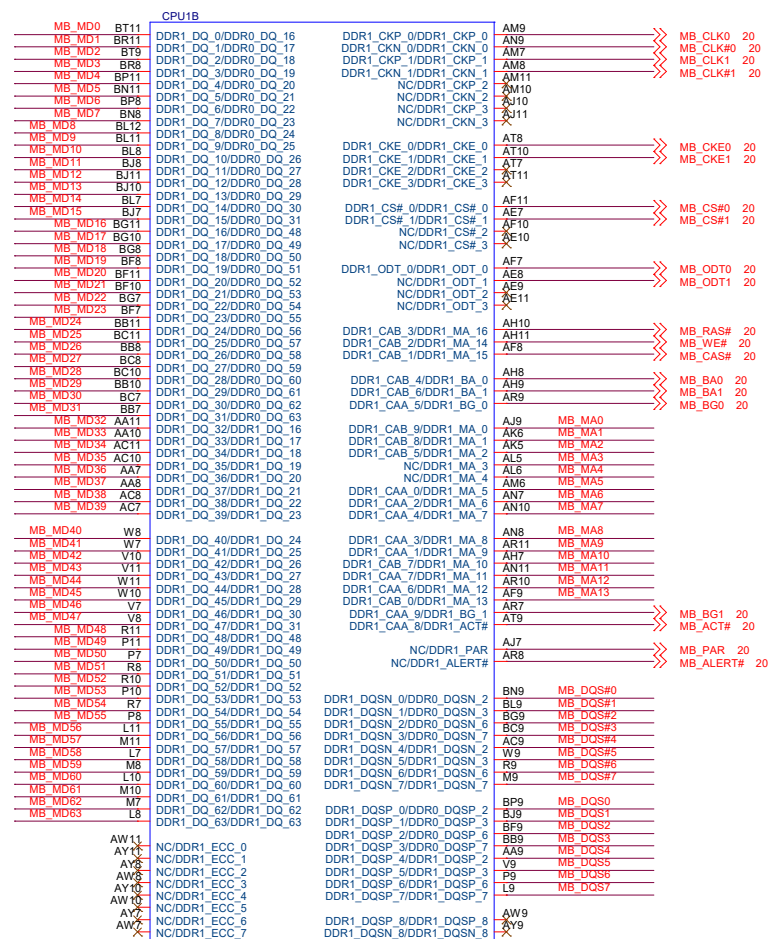
Daughter Board Schematic Version Change List

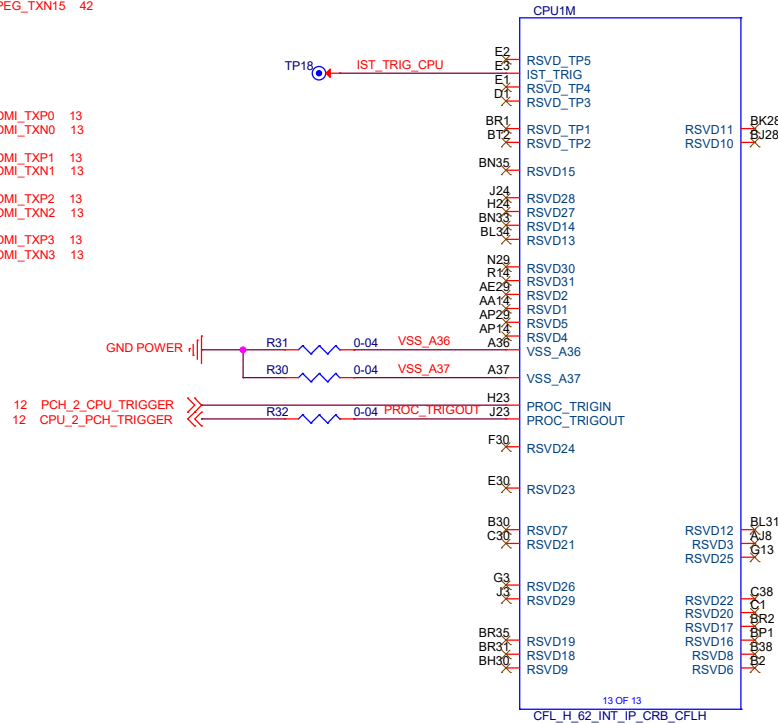
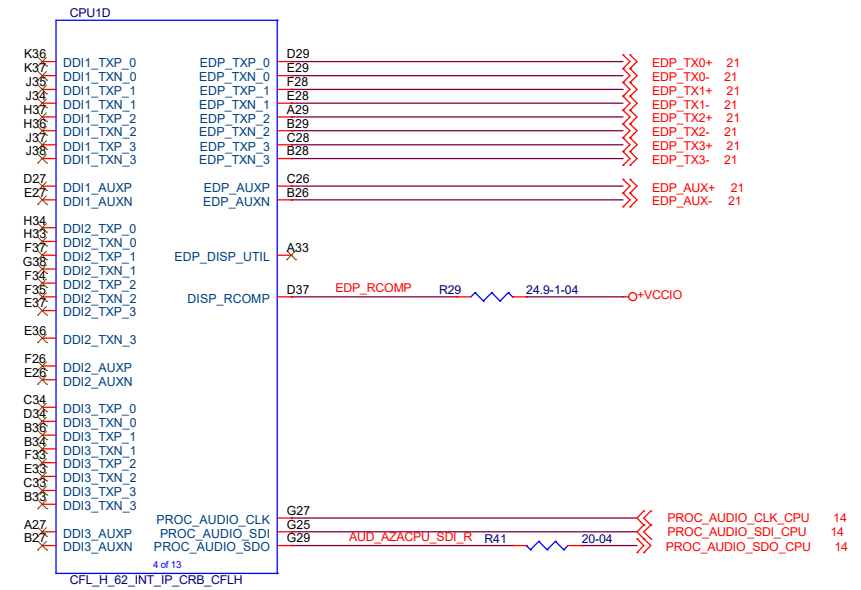
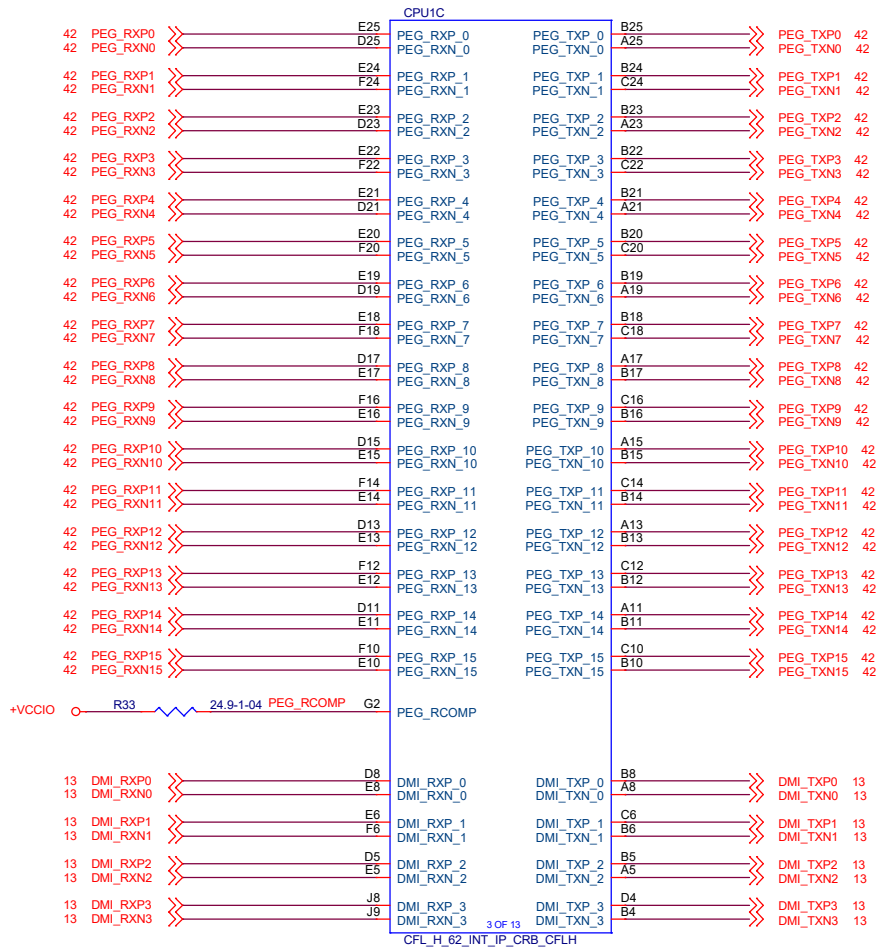
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

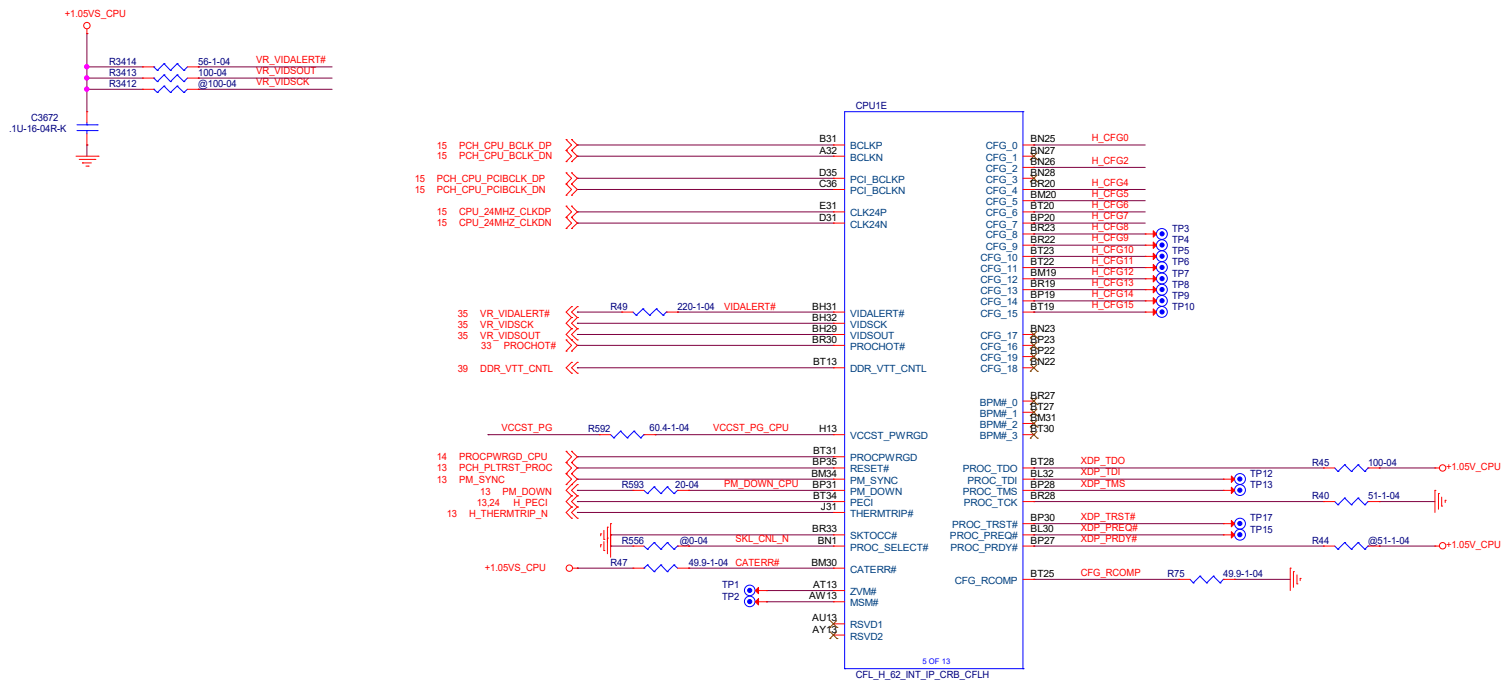
## SYSTEM BLOCK DIAGRAM











H_CFG0 (IPU)	Stall reset sequence after PCU PLL lock until de-asserted
0	Stall
1	Normal Operation : No stall. (Default)

H\_CFG0 R180 @1K-1-04

H_CFG2 (IPU)	PCI Express* Static x16 Lane Numbering Reversal
0	Lane numbers reversed
1	Normal operation

H\_CFG2 R181 1K-1-04

H_CFG4 (IPU)	eDP Presence strap
0	Enabled
1	Disabled

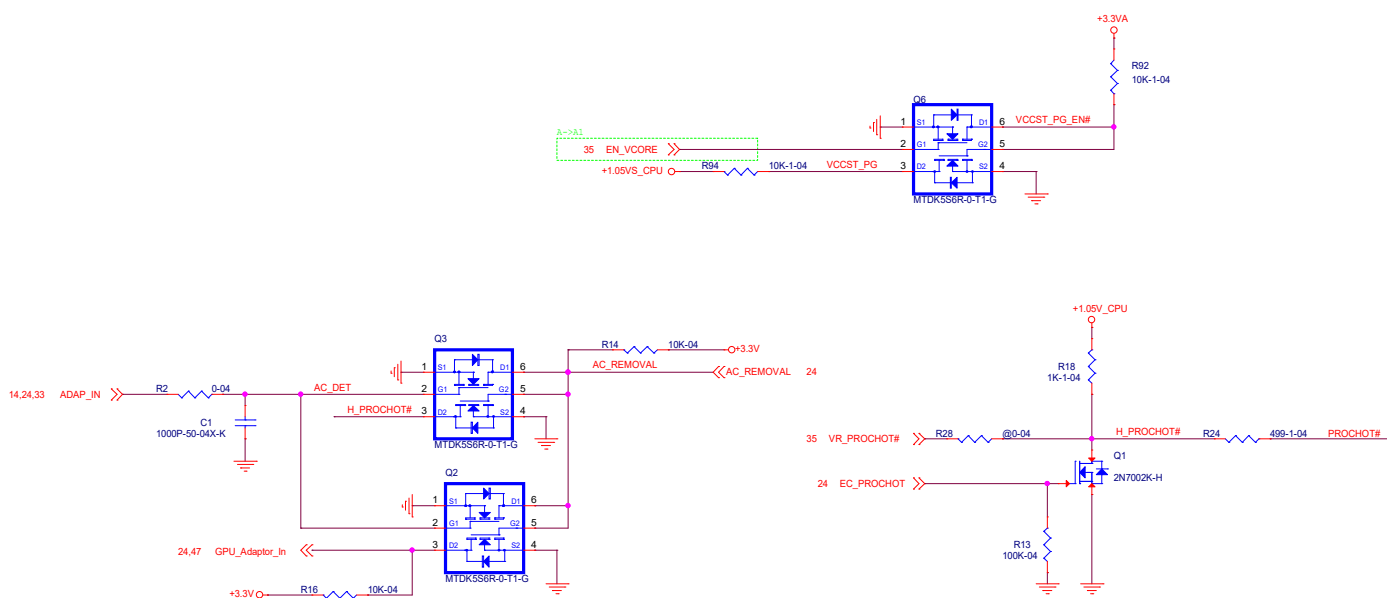
H\_CFG4 R172 1K-1-04

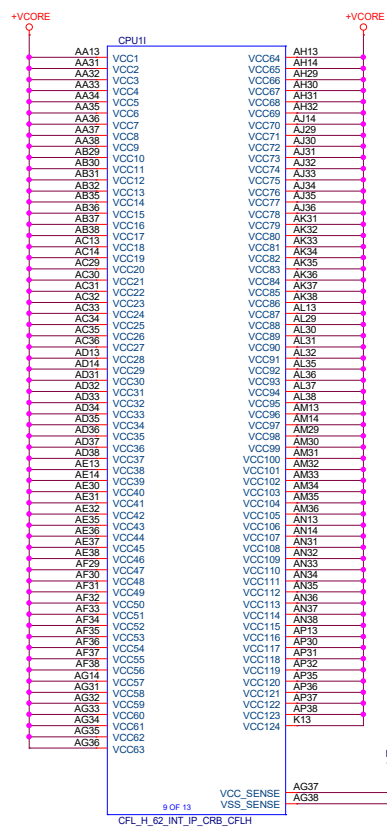
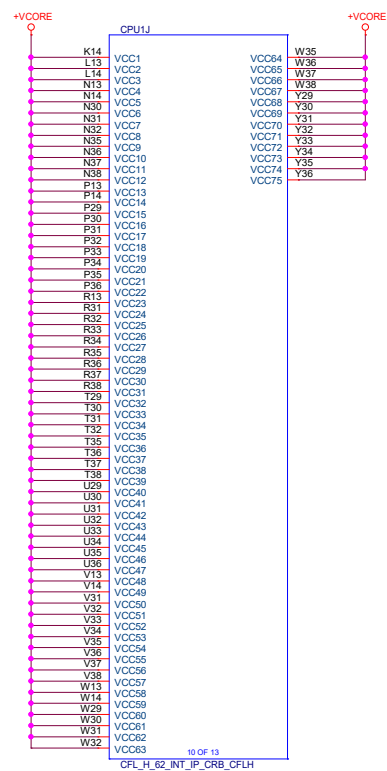
H_CFG6 (IPU)	H_CFG5 (IPU)	PCI Express* Bifurcation
0	0	1 x8, 2 x4 PCI Express
0	1	reserved
1	0	2 x8 PCI Express
1	1	1 x16 PCI Express

H\_CFG5 R174 @1K-1-04  
H\_CFG6 R173 @1K-1-04

H_CFG7 (IPU)	PEG Training
0	PEG Wait for BIOS for training
1	PEG Train immediately following RESET# de assertion (Default)

H\_CFG7 R175 @1K-1-04

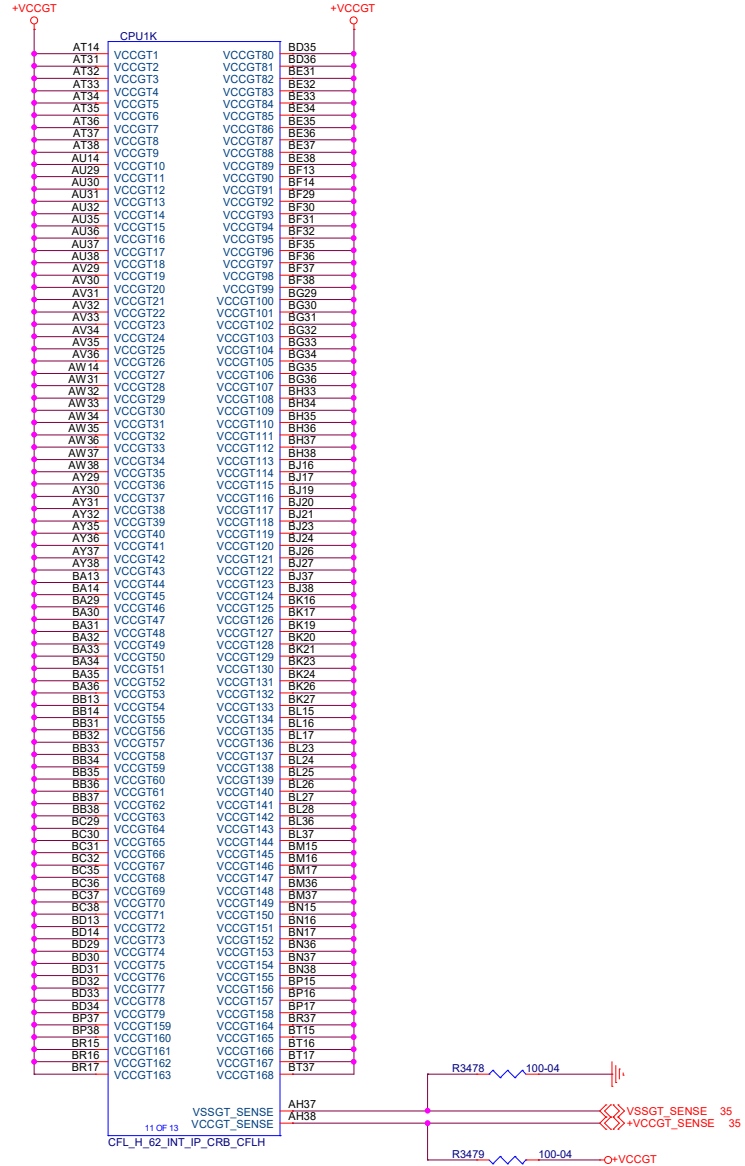
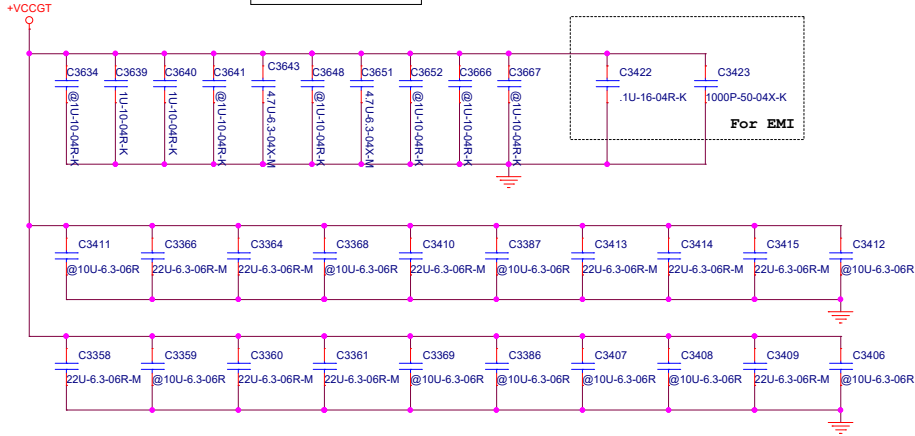




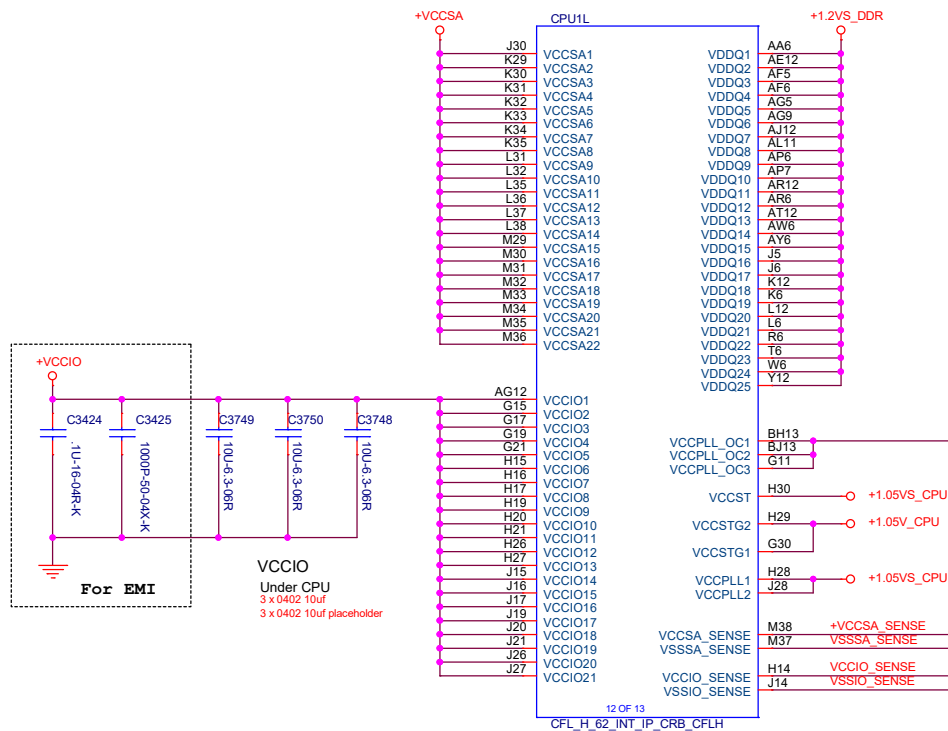
564042\_KBL\_PDG\_V2.0  
VCCGT

Under CPU  
10 x 0402 10uF  
12 x 0201 1uF

Near CPU  
3 x 0805 47uF  
7 x 0603 22uF





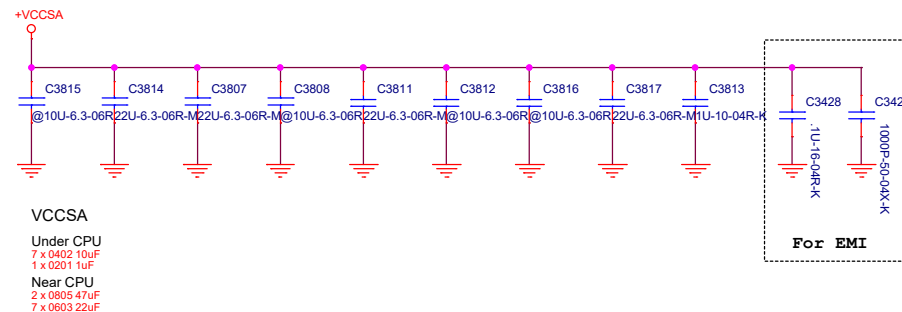
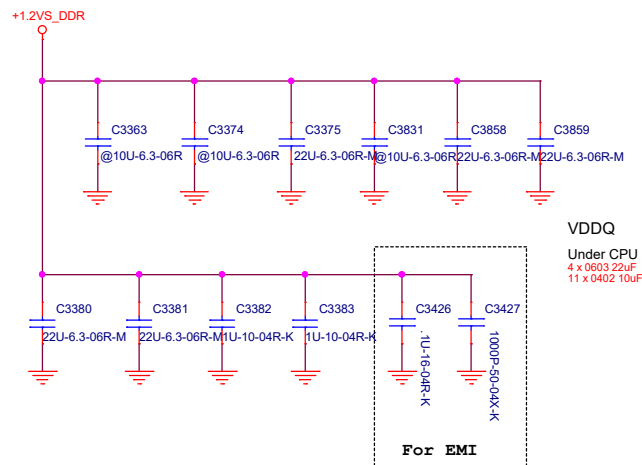


VCCPLL\_OC:  
CPU digital PLL power rails  
VCCPLL:  
CPU PLL power rails

VCCST:  
Sustain voltage for processor  
in Standby modes  
VCCSTG:  
Gated version of VCCST

(1)VCCPLL is allowed to be OFF in S3,  
but it is generally assumed to be ON  
since it is powered from the same  
source as VCCST.

(2) VCCPLL\_OC is allowed to be turned  
off during S3 if it is not powered  
directly from VDDQ



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Title  
**CFL-H VCCSA/VCCIO/VDDQ**

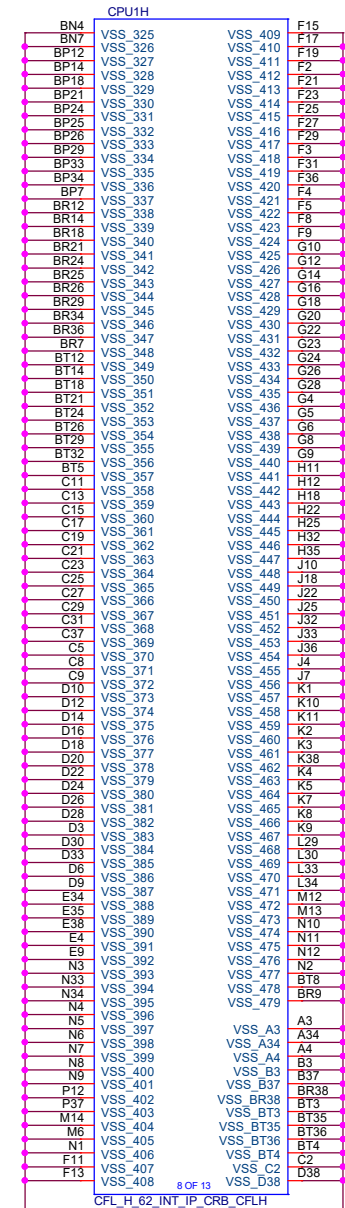
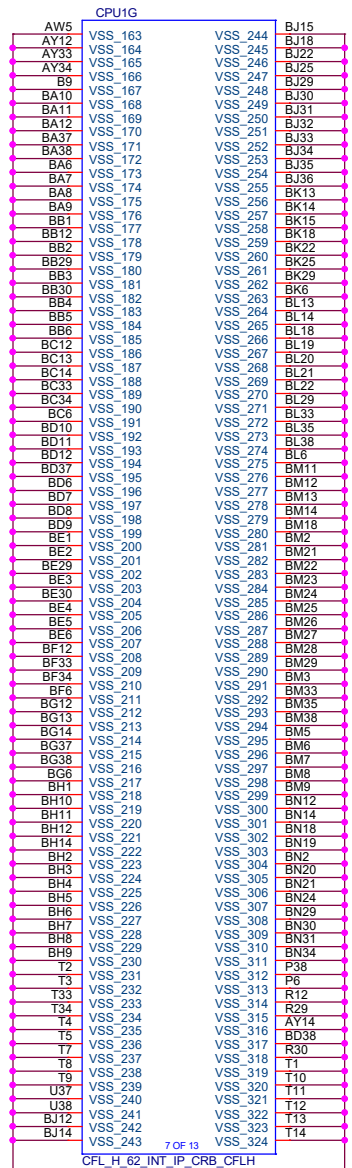
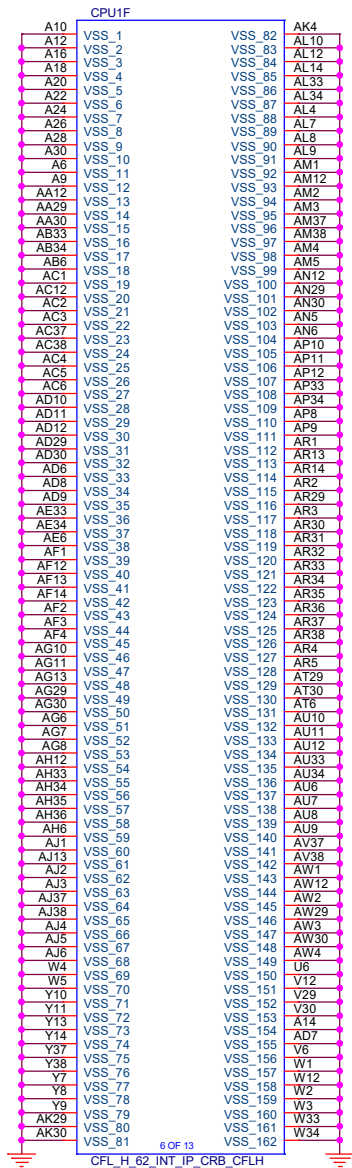
Size  
Custom

Date: Friday, November 16, 2018

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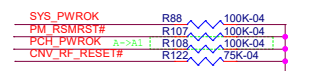
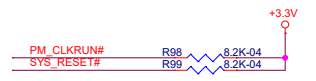
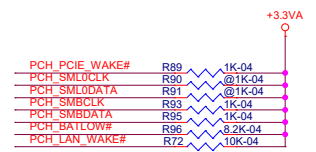
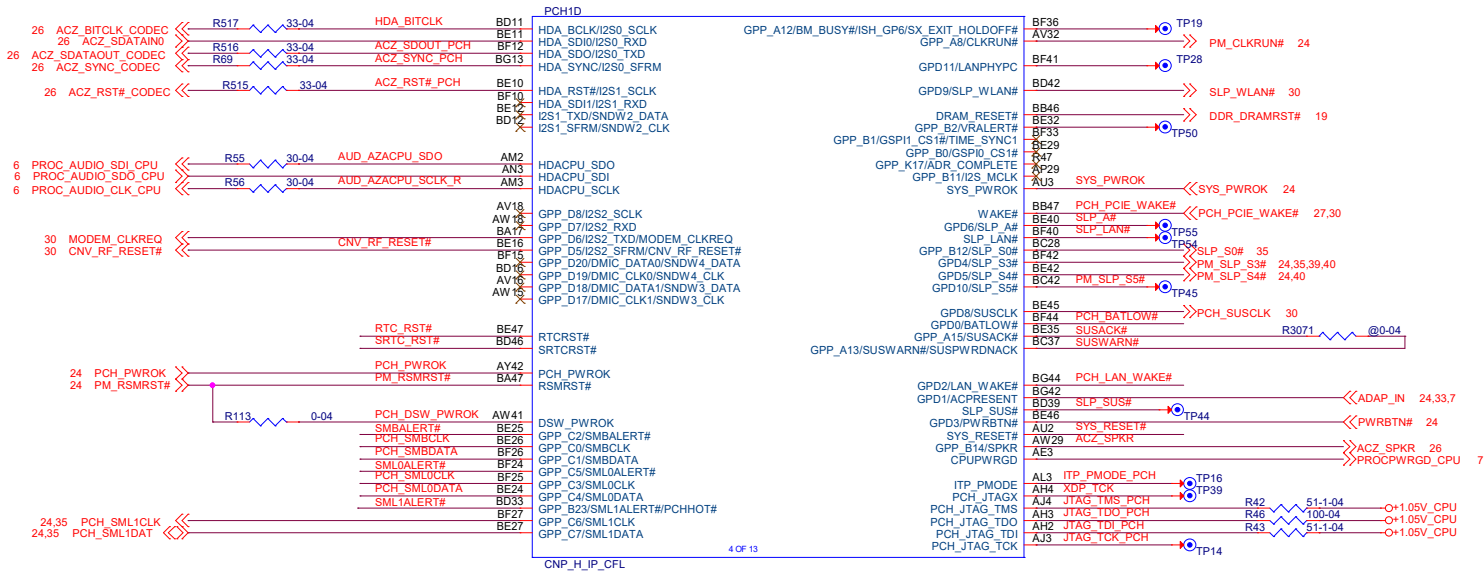
**GK5CN5Z**

Rev  
**B**





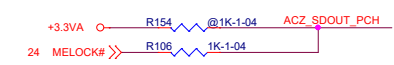




ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable

ACZ\_SPKR R150 @1K-04 +3.3V

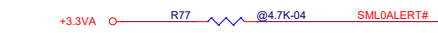
HDA_SDO (IPD)	Flash Descriptor Security Override
0	ME Enable security (Default)
1	ME Disabled security



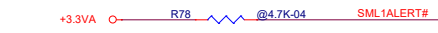
SMBALERT#(IPD)	Intel ME Crypto Transport Layer Security Confidentiality (TLS)
0	Disable (Default)
1	Enable



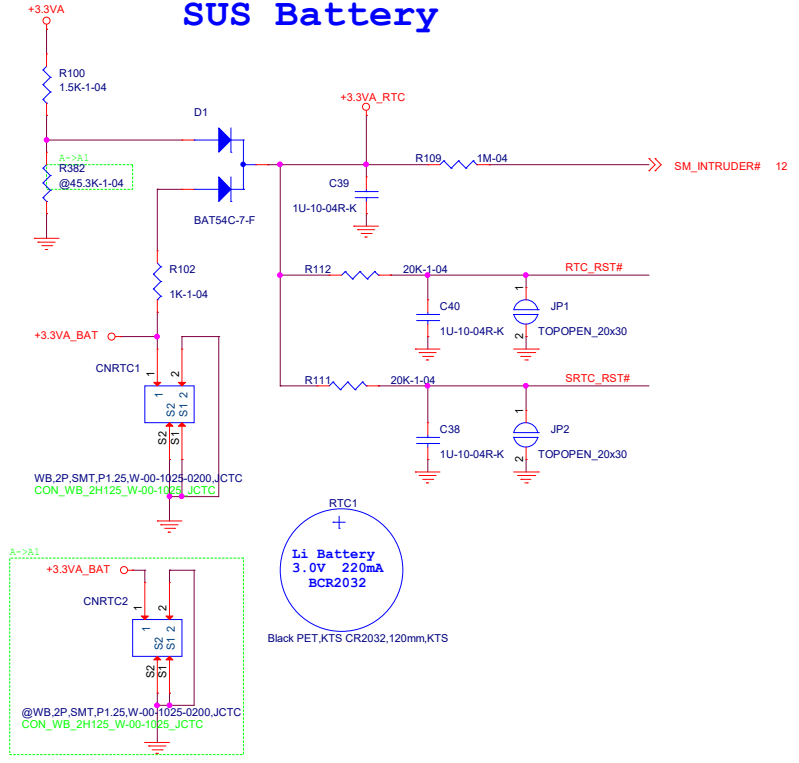
SML0ALERT#(IPD)	eSPI&LPC Select
0	LPC (Default)
1	eSPI



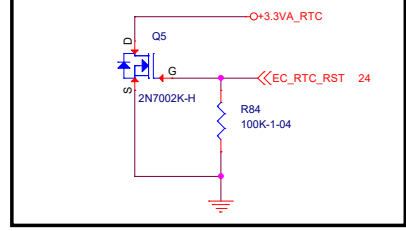
SML1ALERT#(IPD)	IntelR DCI-OOB
0	Disable (Default)
1	Enable



## SUS Battery



## CLEAR CMOS





GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3V<sub>O</sub> R545 @150K-04 PCH\_GSPI1\_SI\_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

+3.3V<sub>O</sub> R546 @4.7K-04 GPP\_B18

CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

A3->B +VCCPRIM\_1P8 R610 4.7K-04 CNV\_BRI\_DT\_PCH

CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

A3->B +VCCPRIM\_1P8 R613 20K-04 CNV\_RGI\_DT\_PCH  
R617 @100K-04

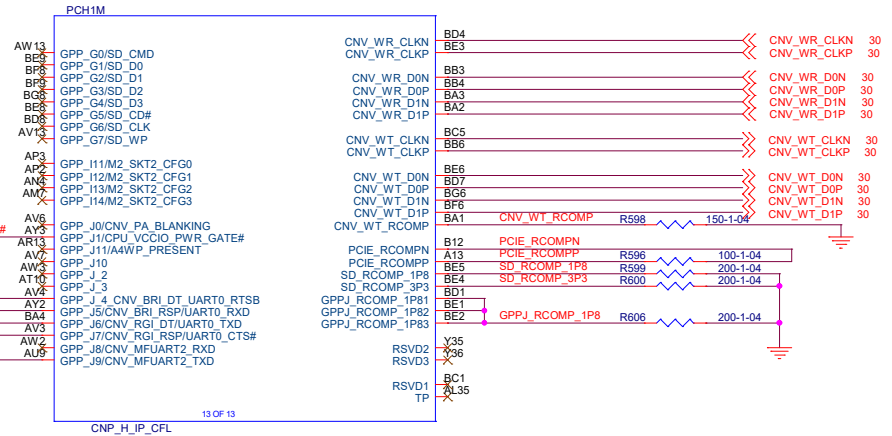
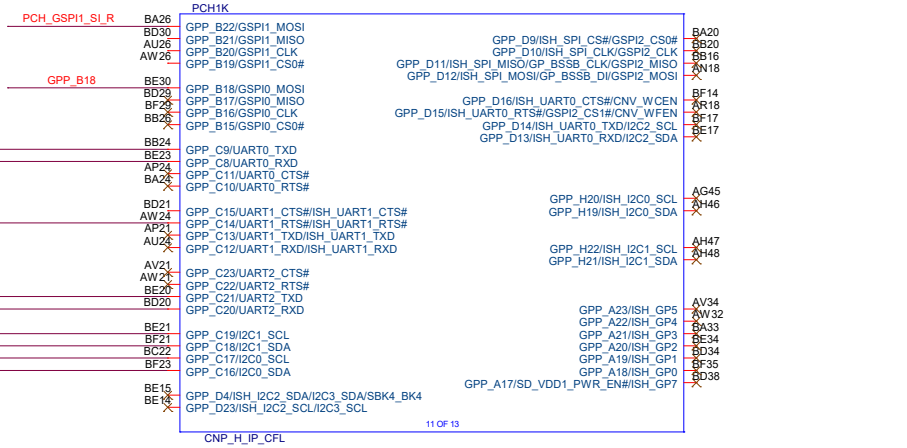
GPP_J9	VCCPSPI Rail select
0	VCCPSPI is connected to 3.3V
1	VCCPSPI is connected to 1.8V

A3->B +VCCPRIM\_1P8 R611 @4.7K-04 GPP\_J9

24 SMC\_WAKE\_SC#  
54,55 FBVDDQ\_PG\_1V8Aon\_GC6

53.54 Dgpu\_PWR\_ON

30 UART2\_DEBUG\_TXD  
30 UART2\_DEBUG\_RXD  
47 CPU\_EVENT#\_GC6  
42 DGPU\_RST#  
31 TP\_I2C0\_SCL  
31 TP\_I2C0\_SDA



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Title CFL-H CNV/UART/I2C

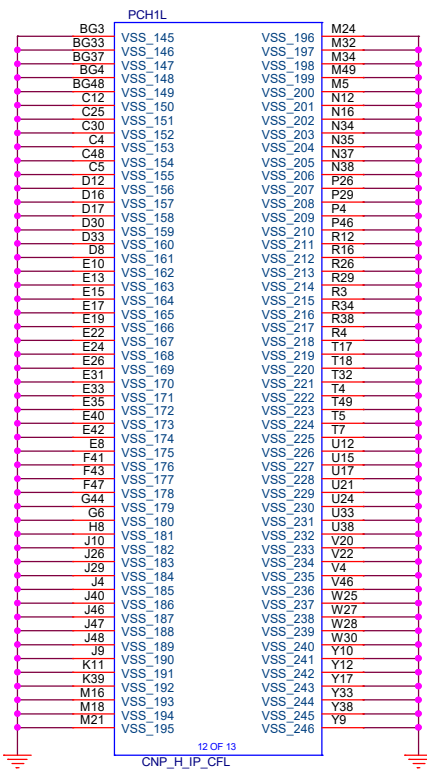
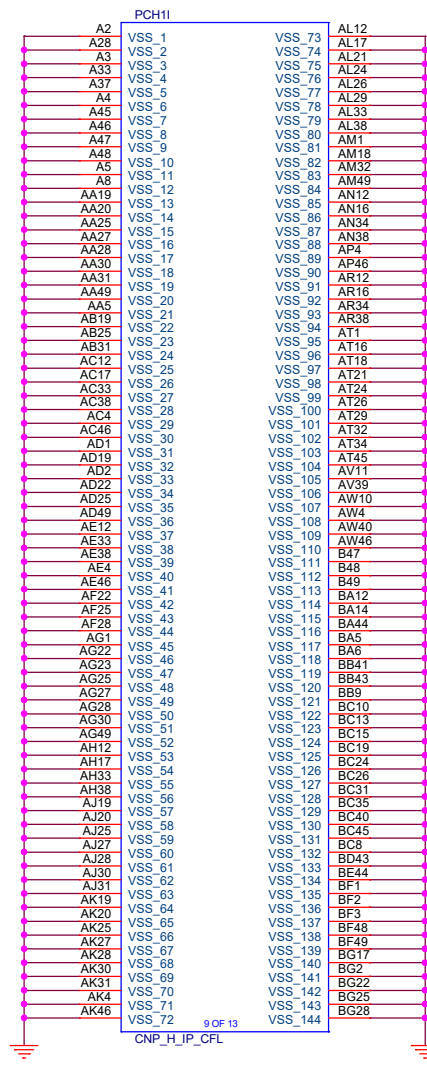
Size Custom Document Number GK5CN5Z Rev B

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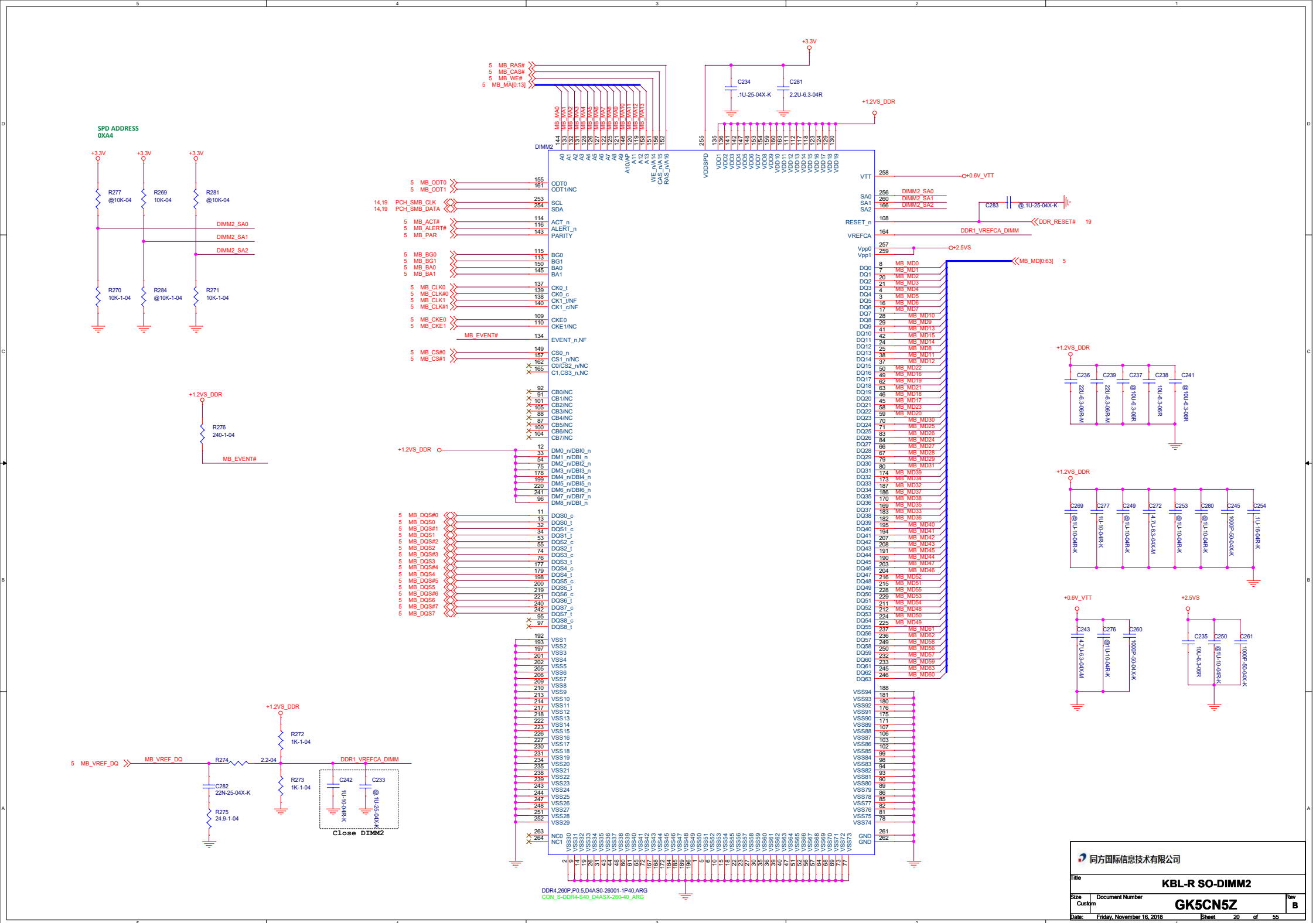




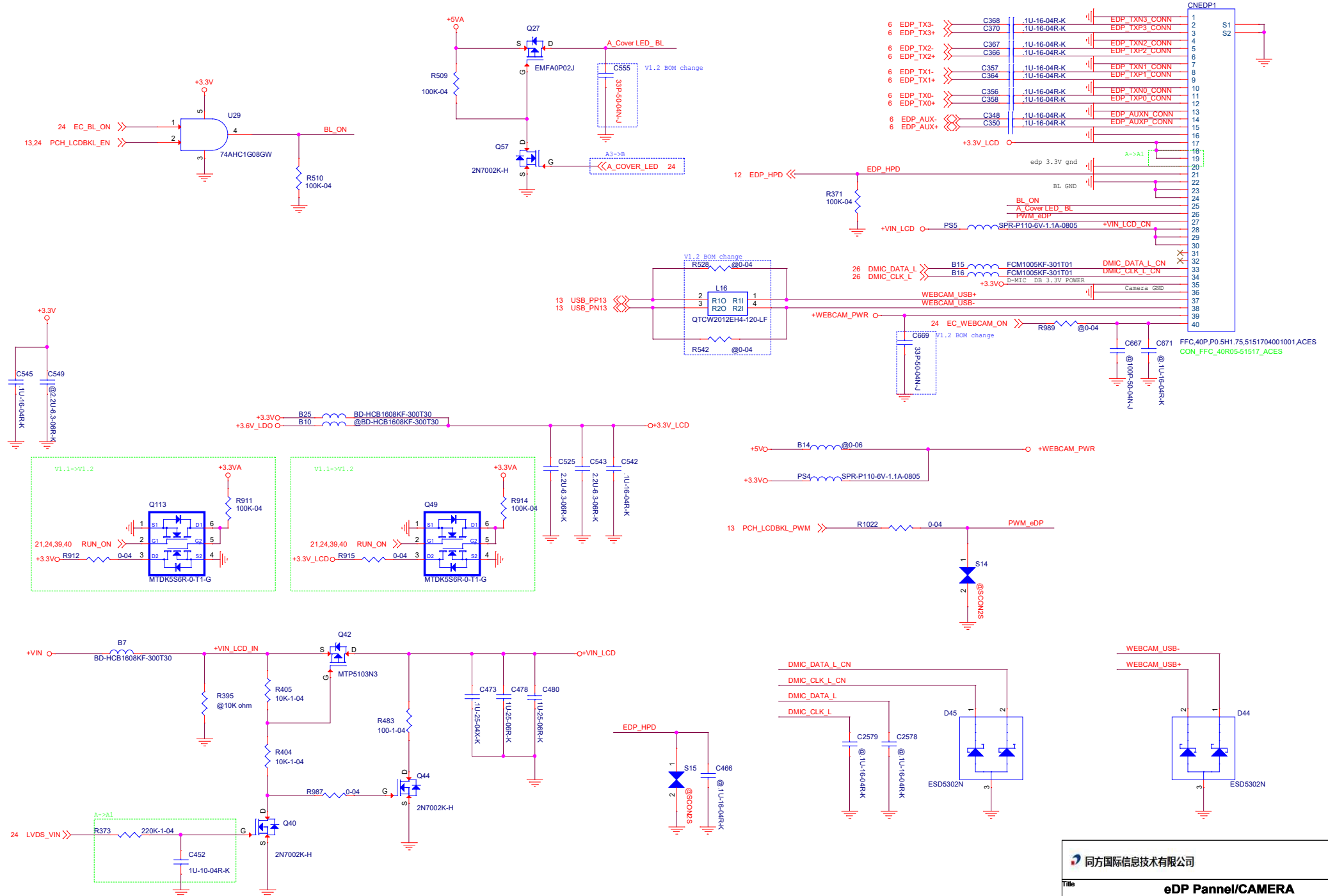








EMFA0P02J MOS SPEC  
ID=-3A, 100 miniOHM@Pulse width=300us



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Title eDP Panel/CAMERA

Size Custom Document Number

GK5CN5Z

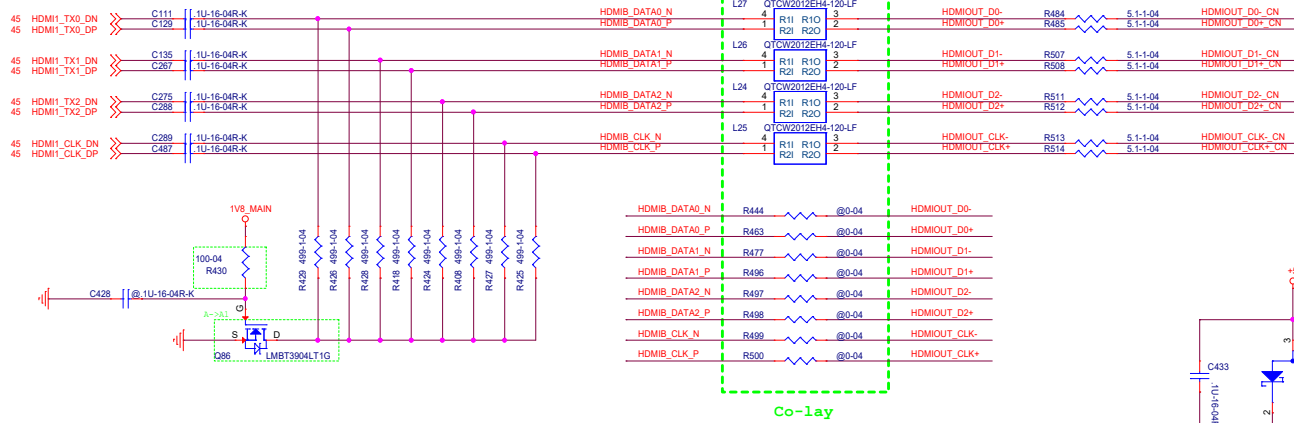
Rev B

Date: Friday, November 16, 2018

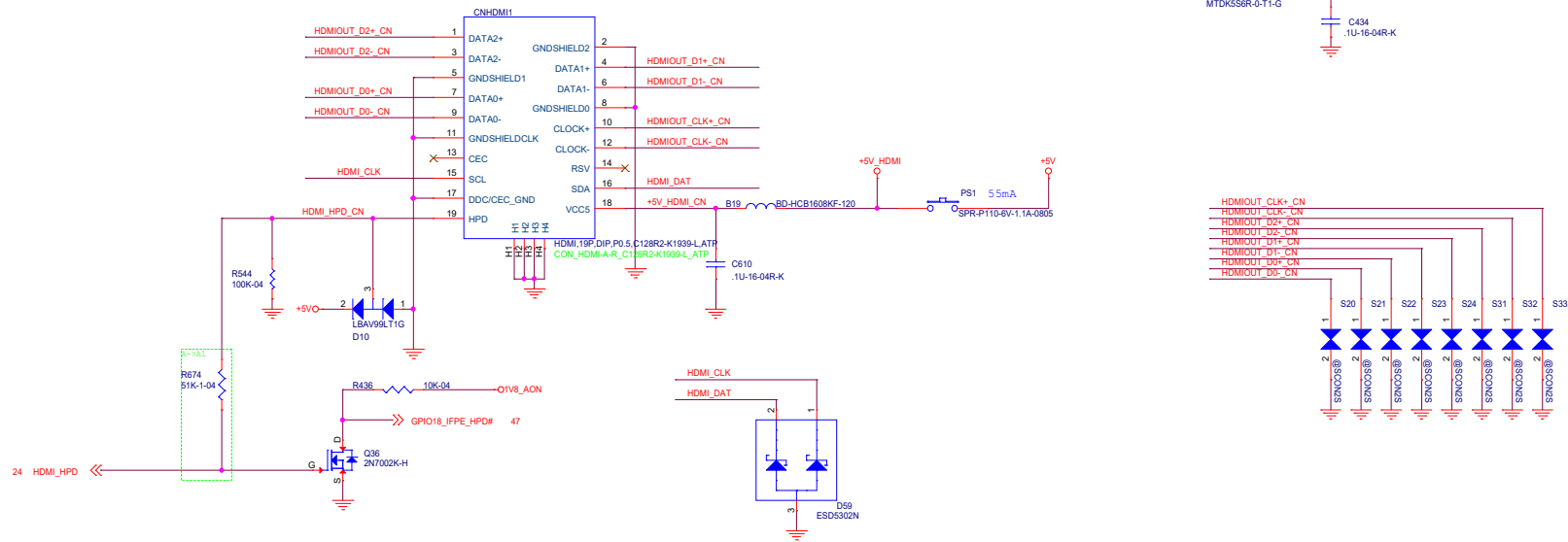
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HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported  
HDMI R1.4 340MHz Intel Supported



## HDMI CONN

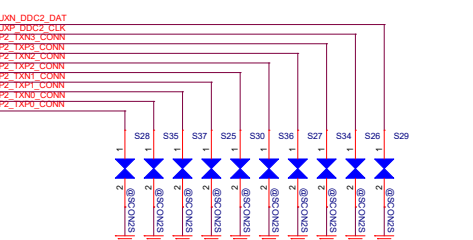
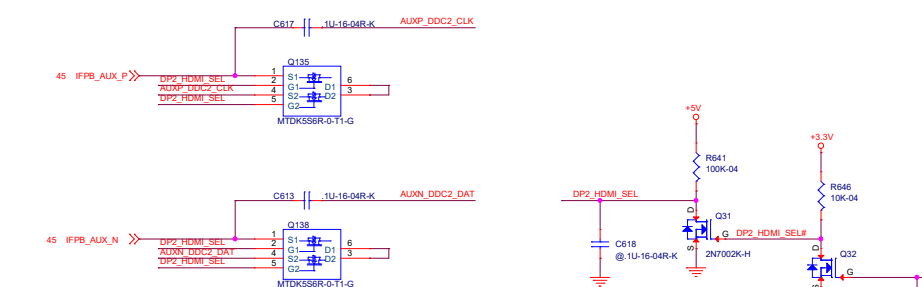
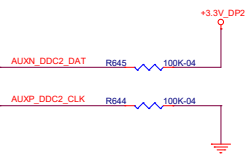
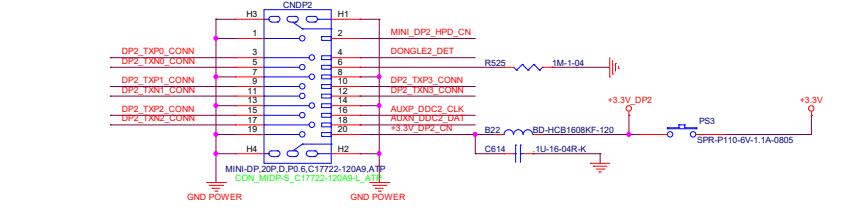
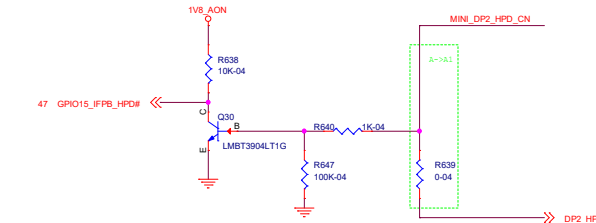
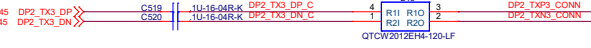
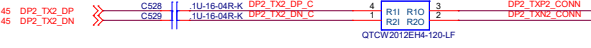
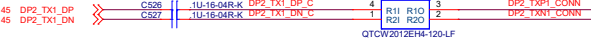
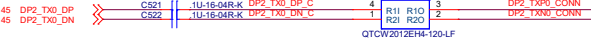
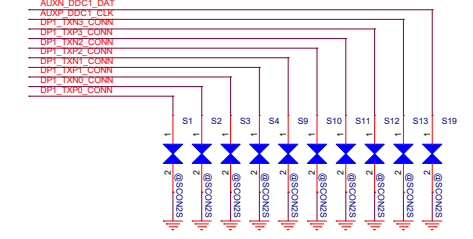
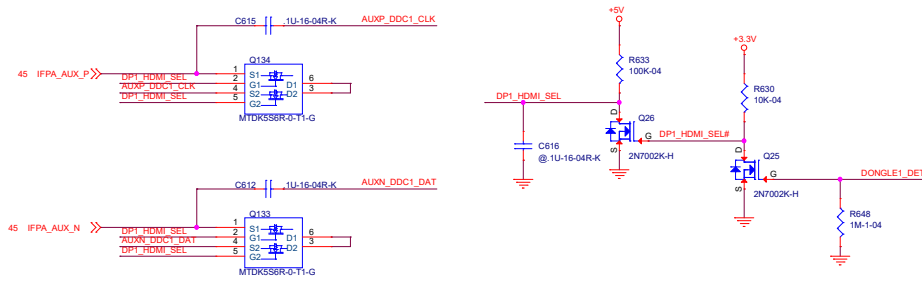
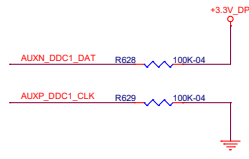
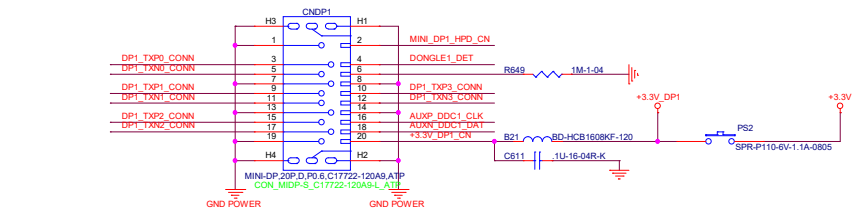
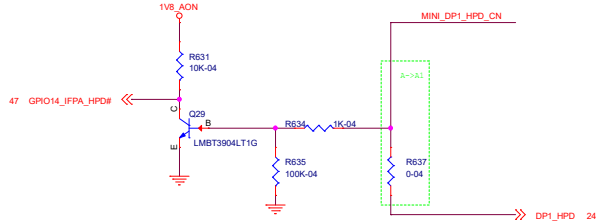
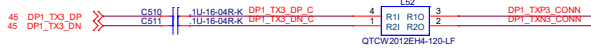
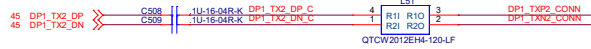
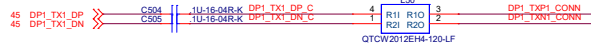
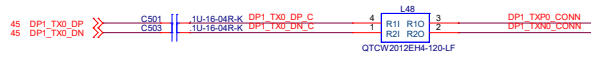


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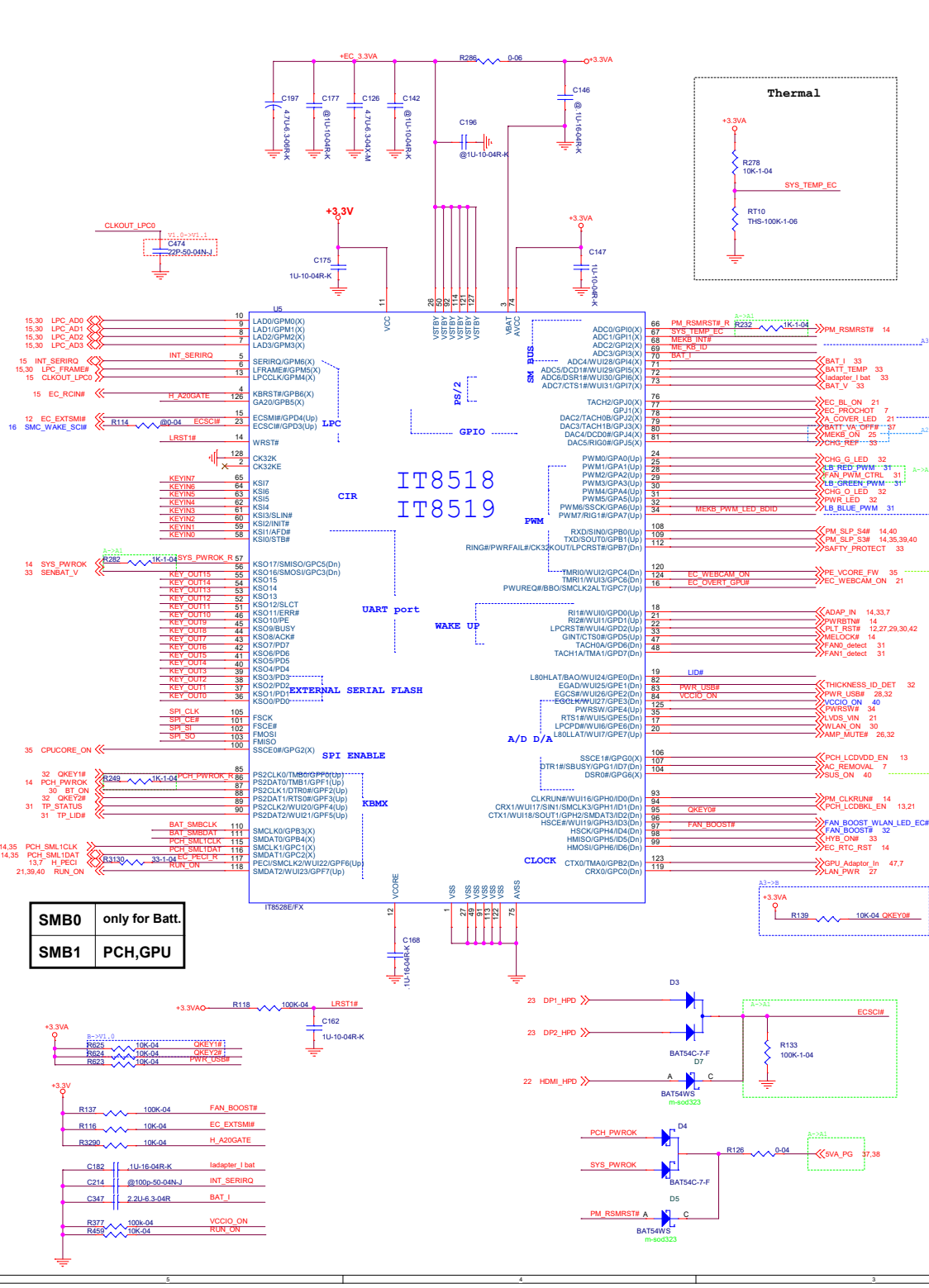
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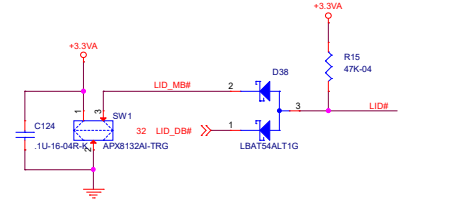
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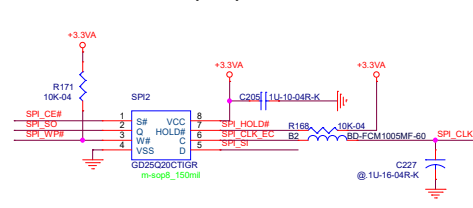
同方国际信息技术有限公司



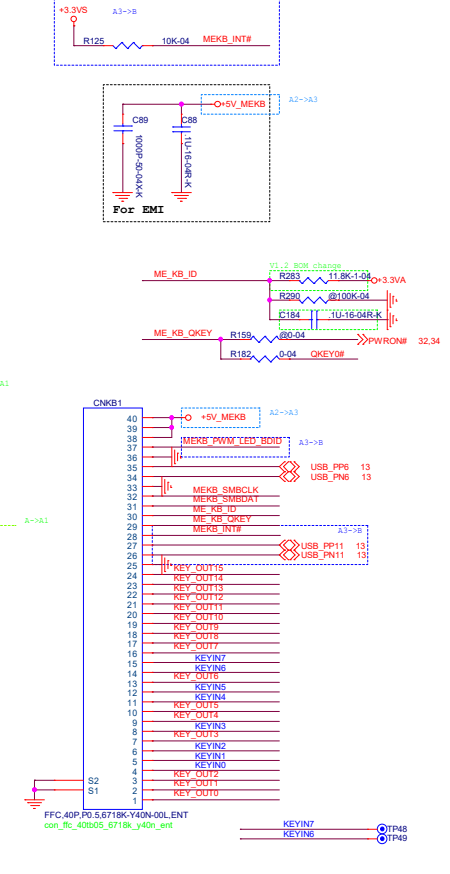
### LID SW



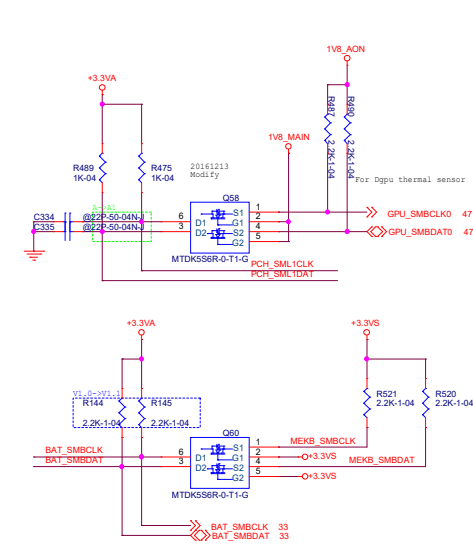
### EC FLASH ROM(SPI)



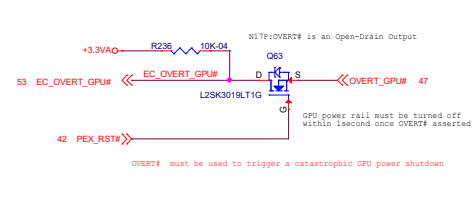
### ME KEYBOARD & 4 AREA KEYBOARD



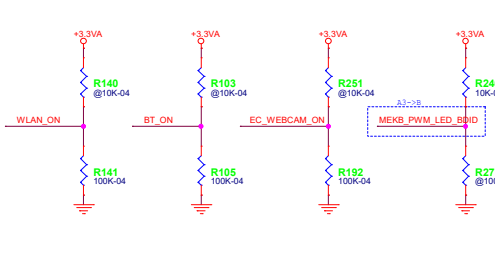
### EC SMBUS LEVEL SHIFT



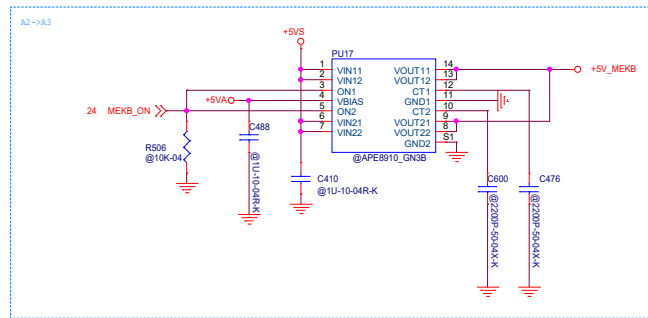
### GPU Over Temperature Protection



### Platform ID

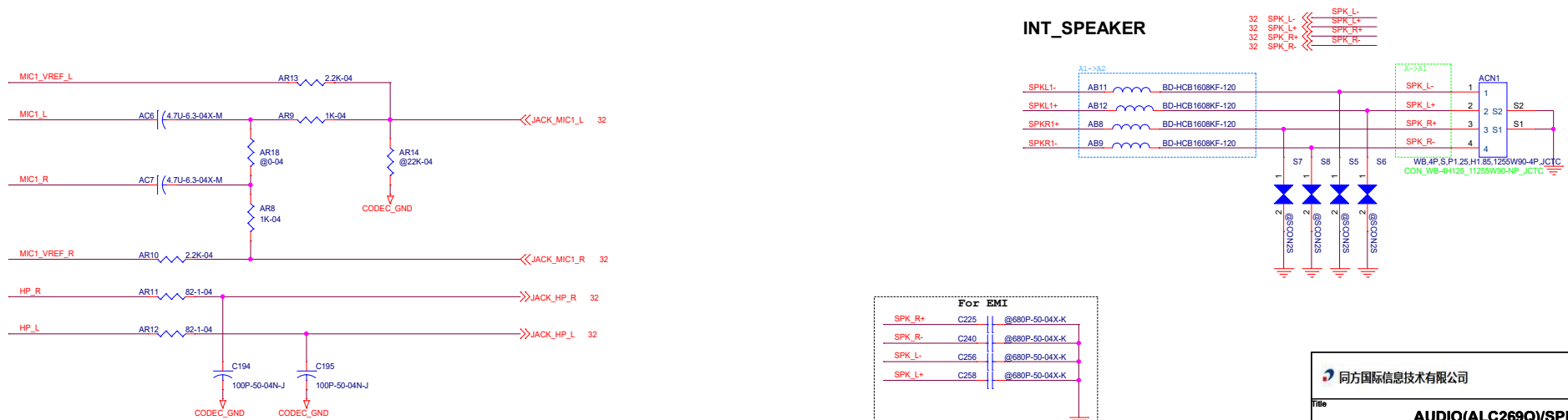
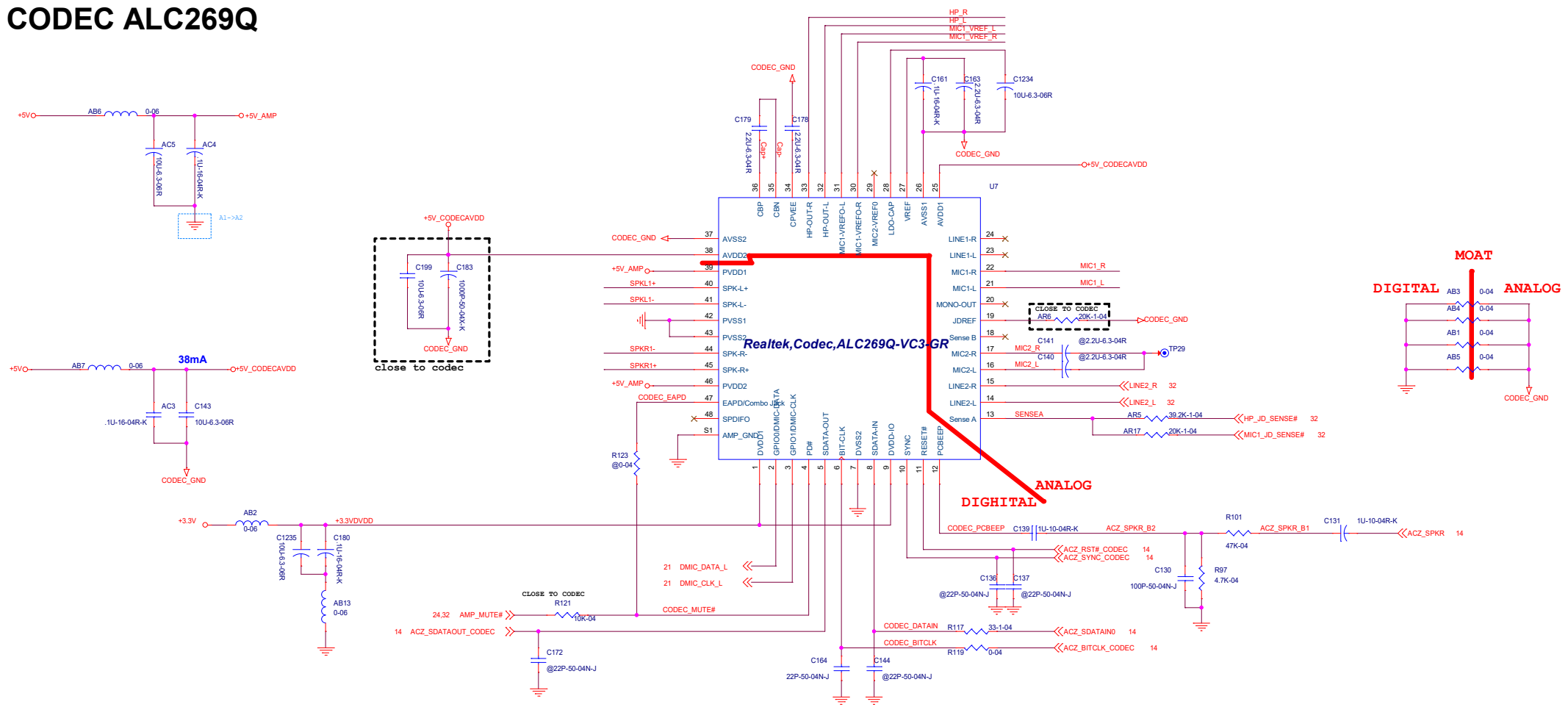


NET	WLAN_ON	BT_ON	EC_WEBCAM_ON	Board ID
HIGH			GR5CN6Z	
LOW	15"	CFL-H	GR5CN5Z	





## CODEC ALC269Q

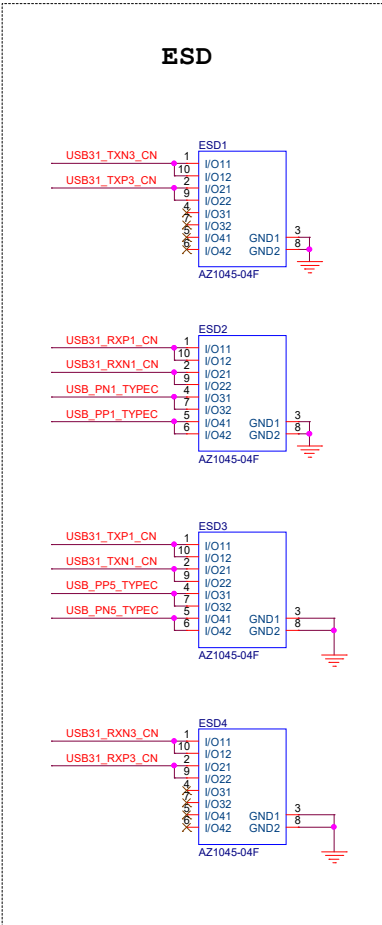
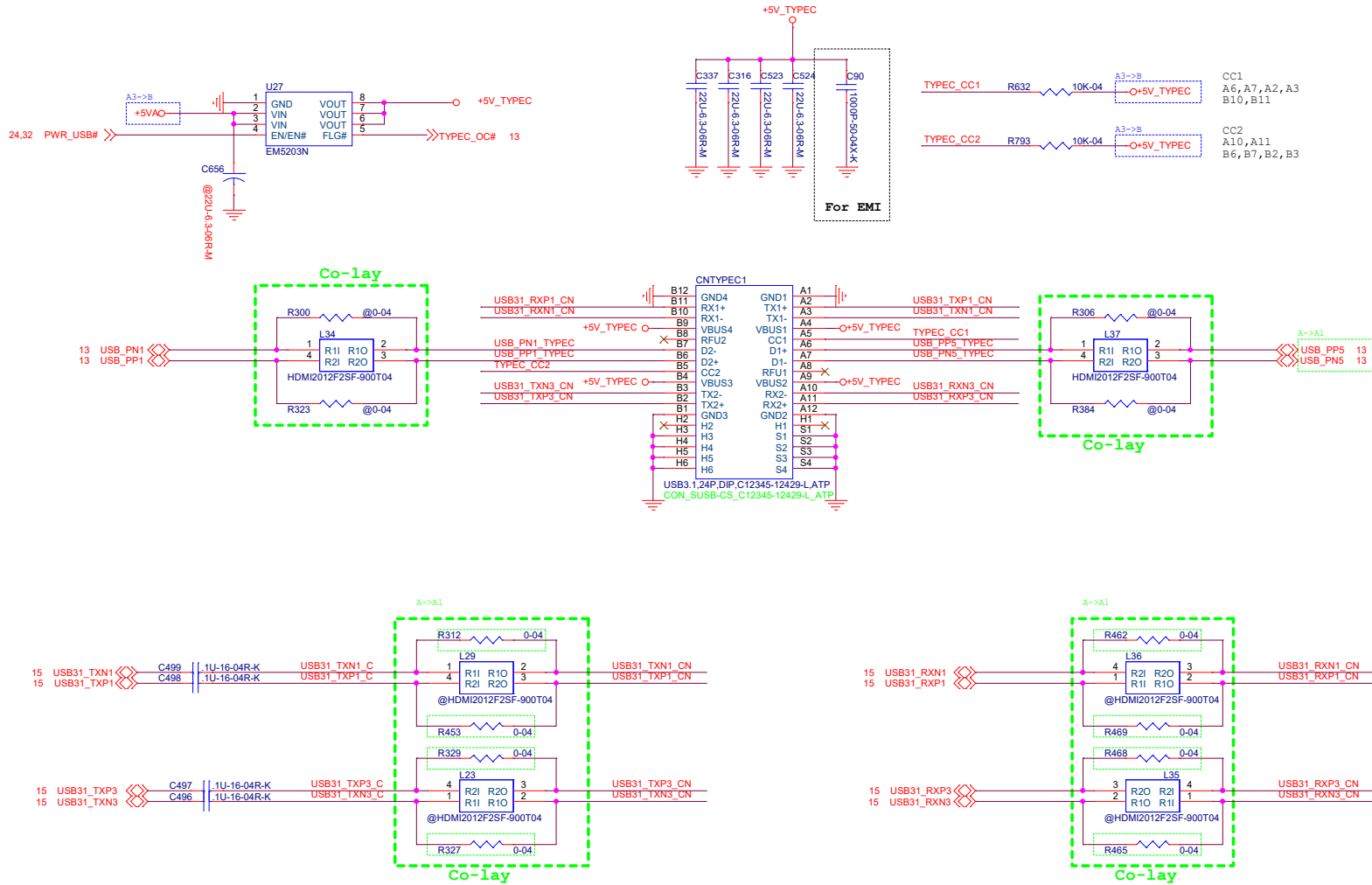


**For EMI**

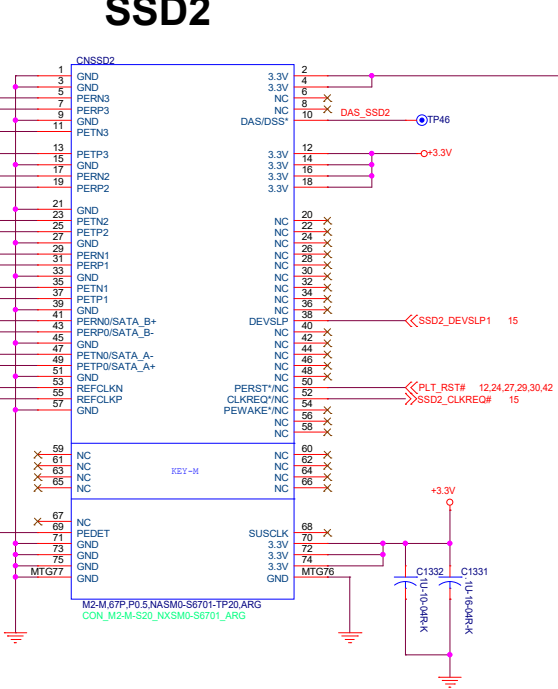
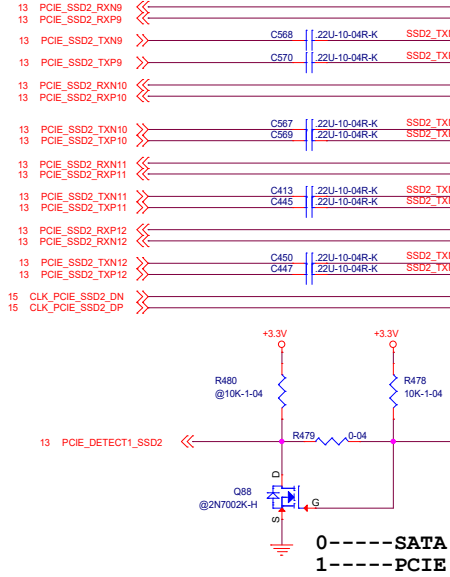
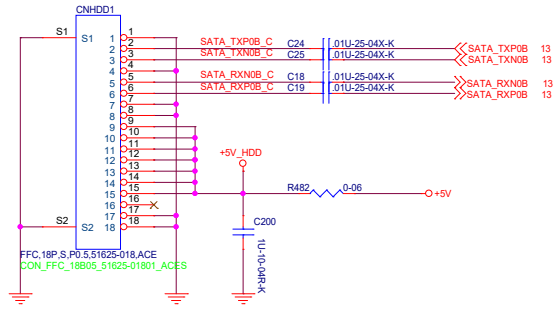
SPK_R+	C225	@680P-50-04X-K
SPK_R-	C240	@680P-50-04X-K
SPK_L-	C256	@680P-50-04X-K
SPK_L+	C258	@680P-50-04X-K



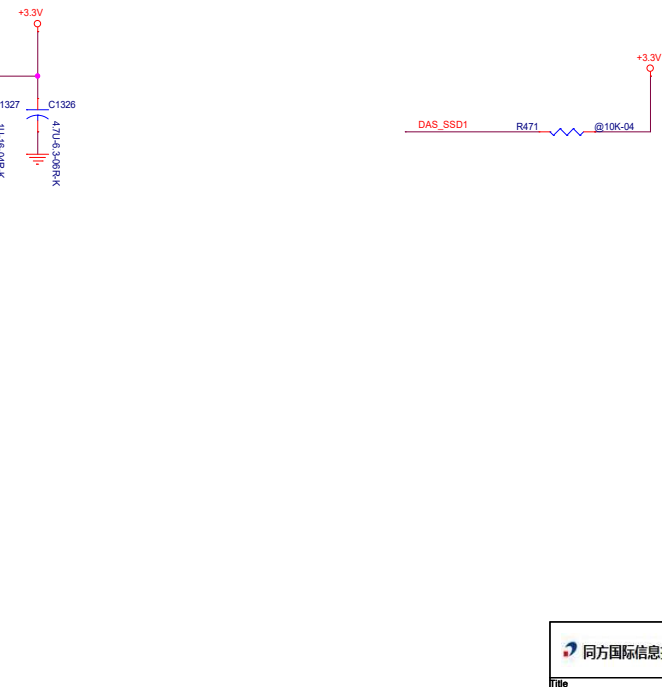
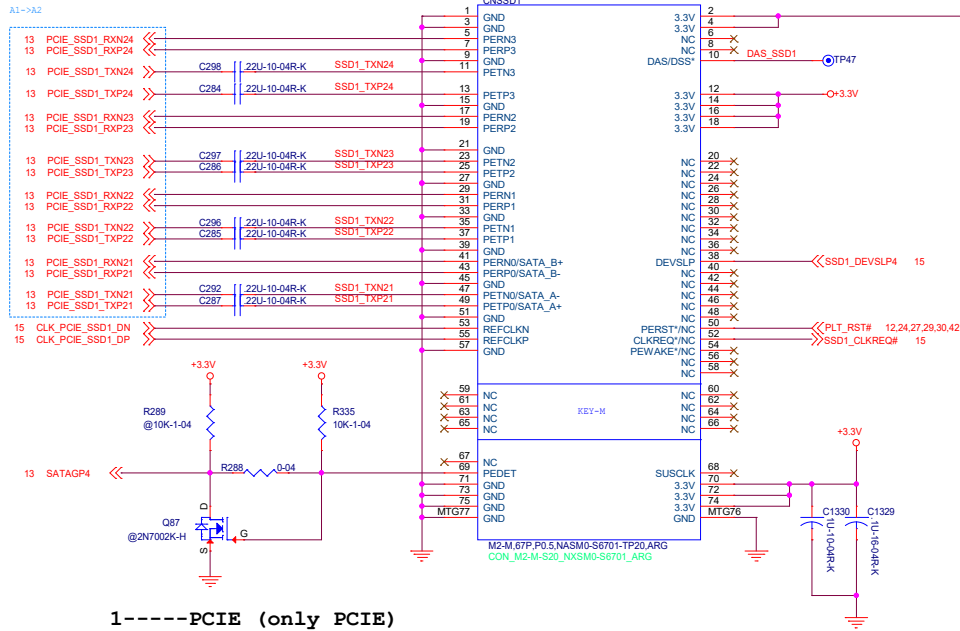
USB3.0 TYPE-C



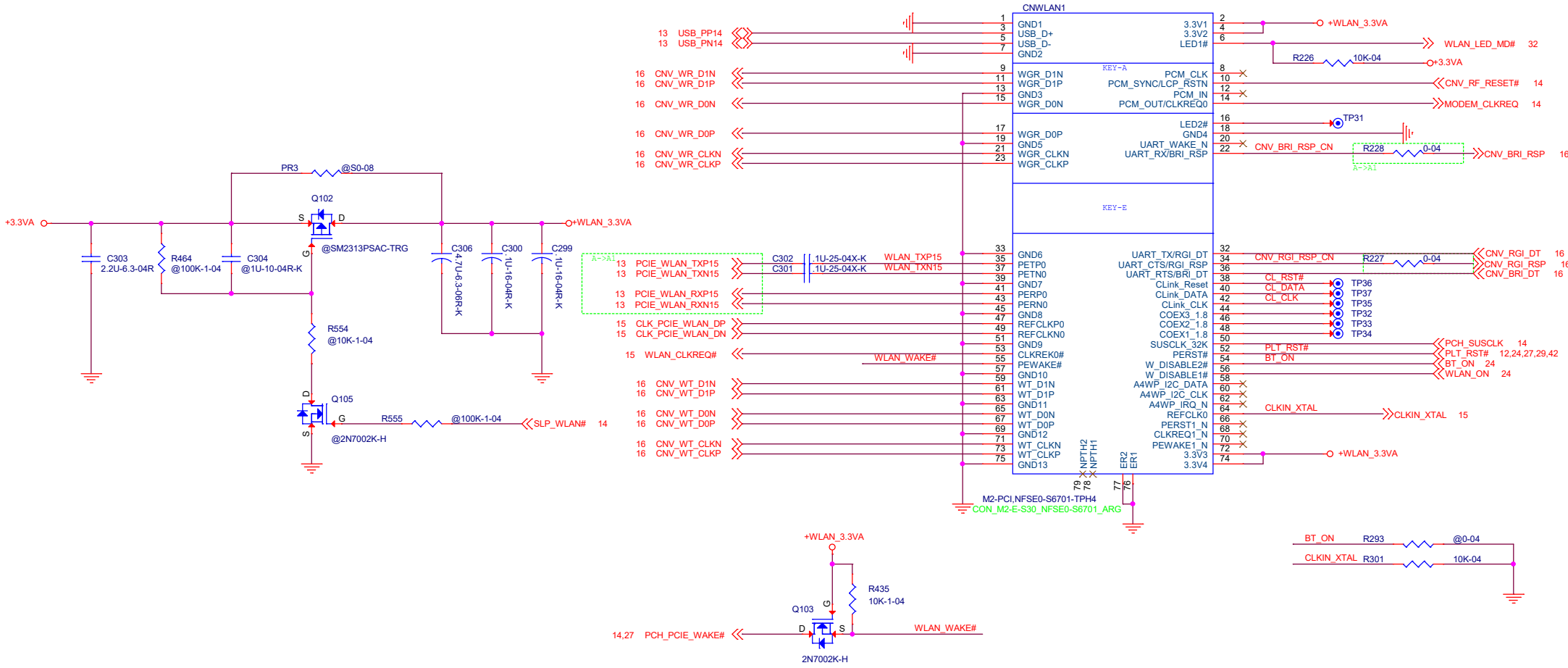
## SATA-HDD



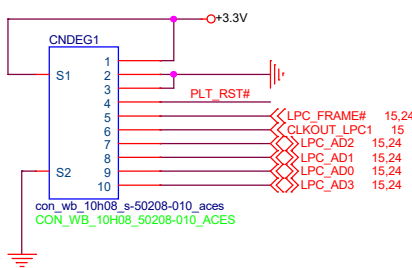
## SSD1



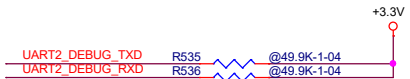
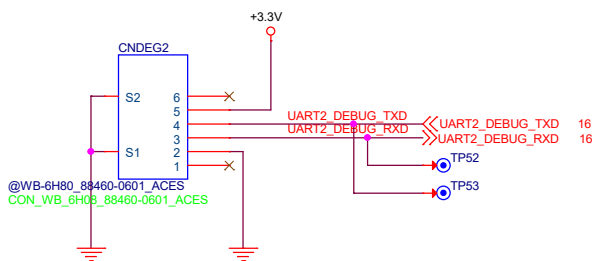
WLAN CONN



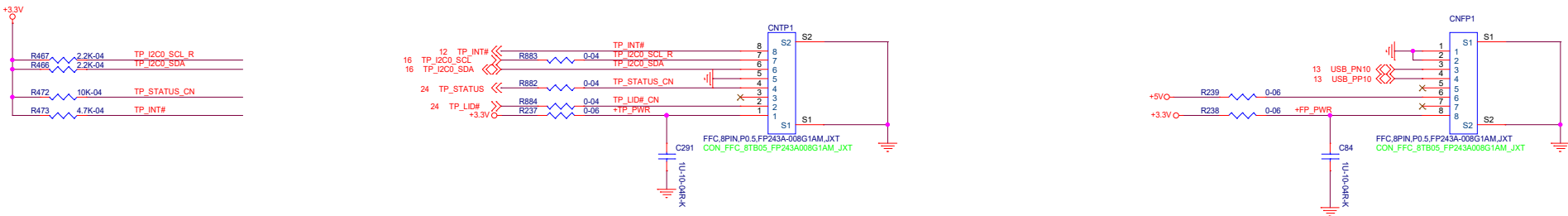
LPC debug port



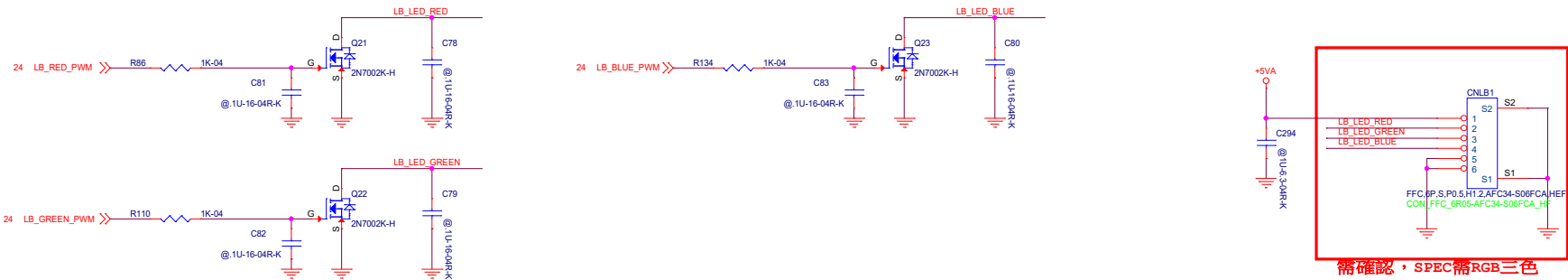
UART debug port



Touch Pad&Finger Print

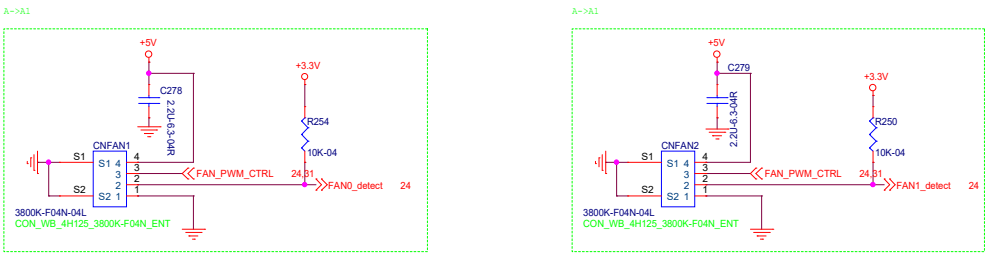


Light bar Control

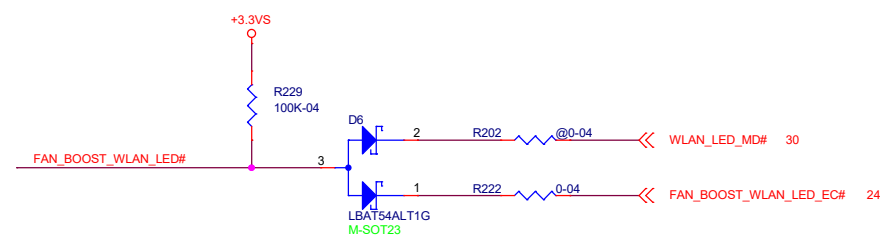
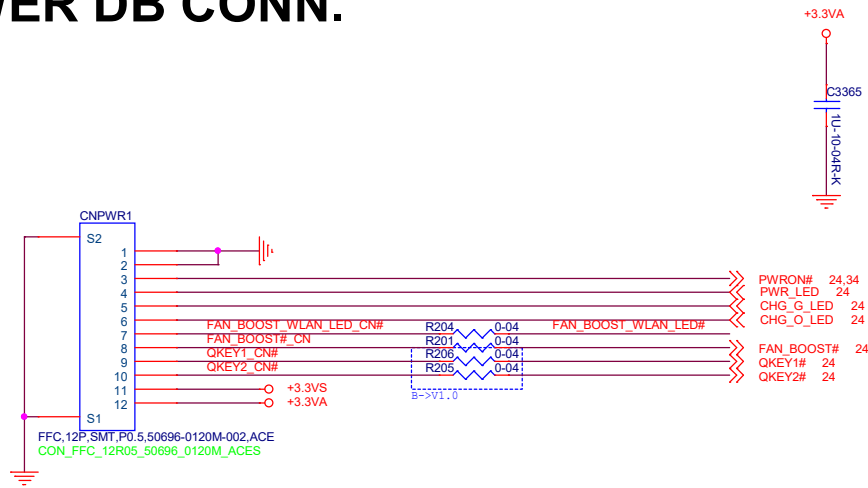


需確認，SPEC需RGB三色

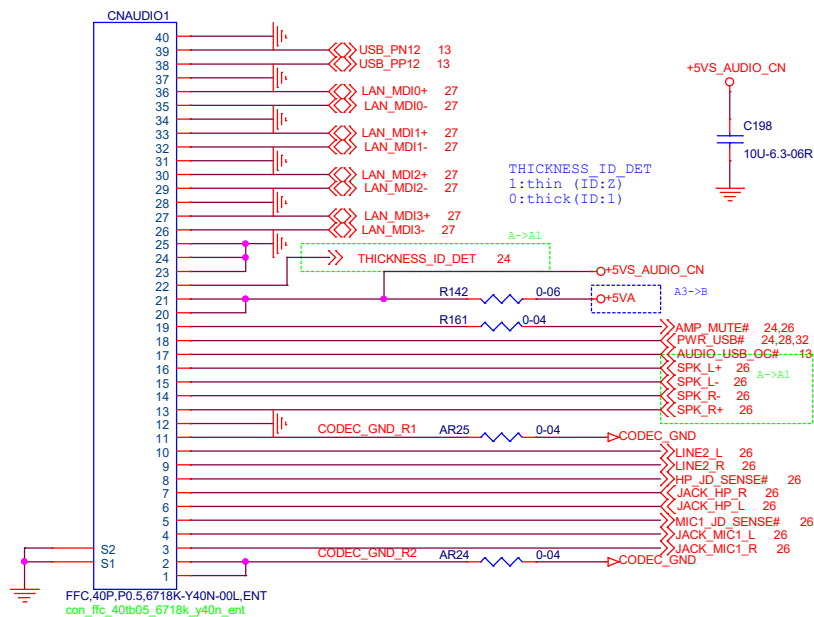
FAN CONTROLLER



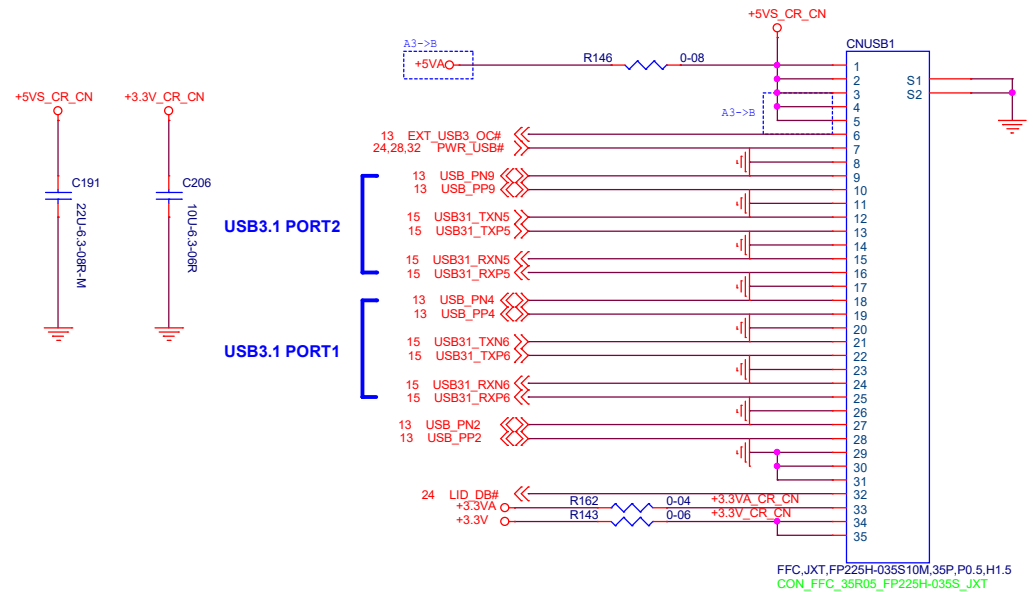
# POWER DB CONN.



# Audio&LAN DB CONN.



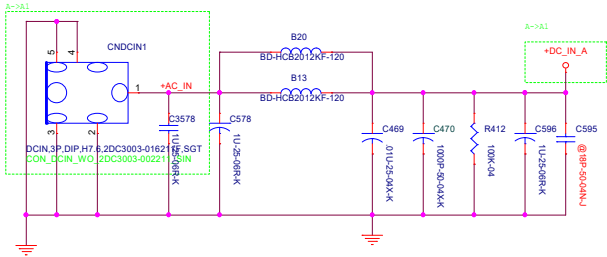
# USB3.0 DB CONN.





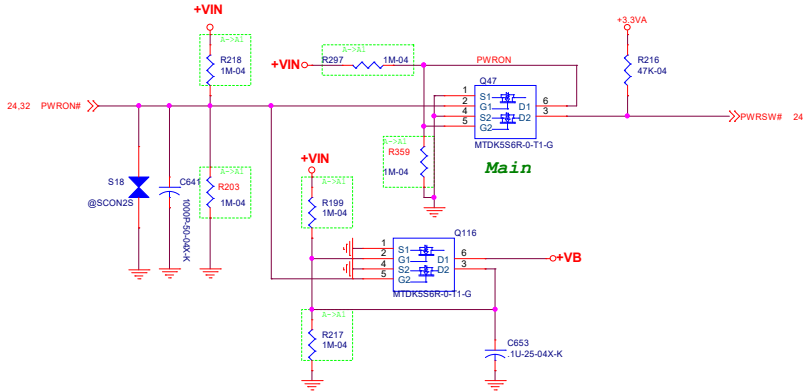


+DC\_IN

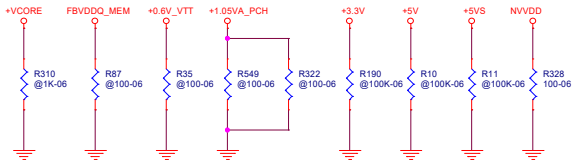


EMB20NP3V  
ID=-13A TC=100 deg  
Ipulse=-72A  
Avalanche=-10A  
9Watt 1ms  
15Watt 0.1ms

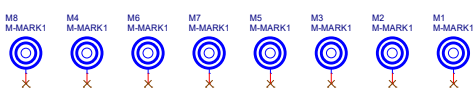
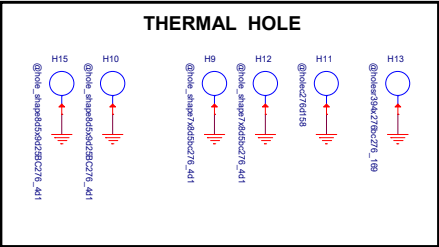
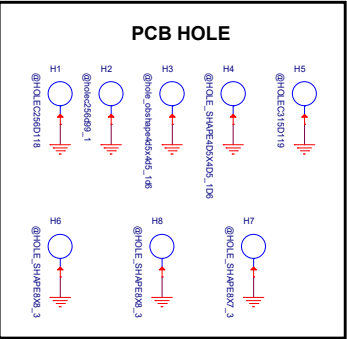
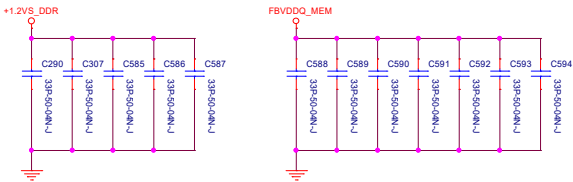
POWER SW



Discharge Resistor

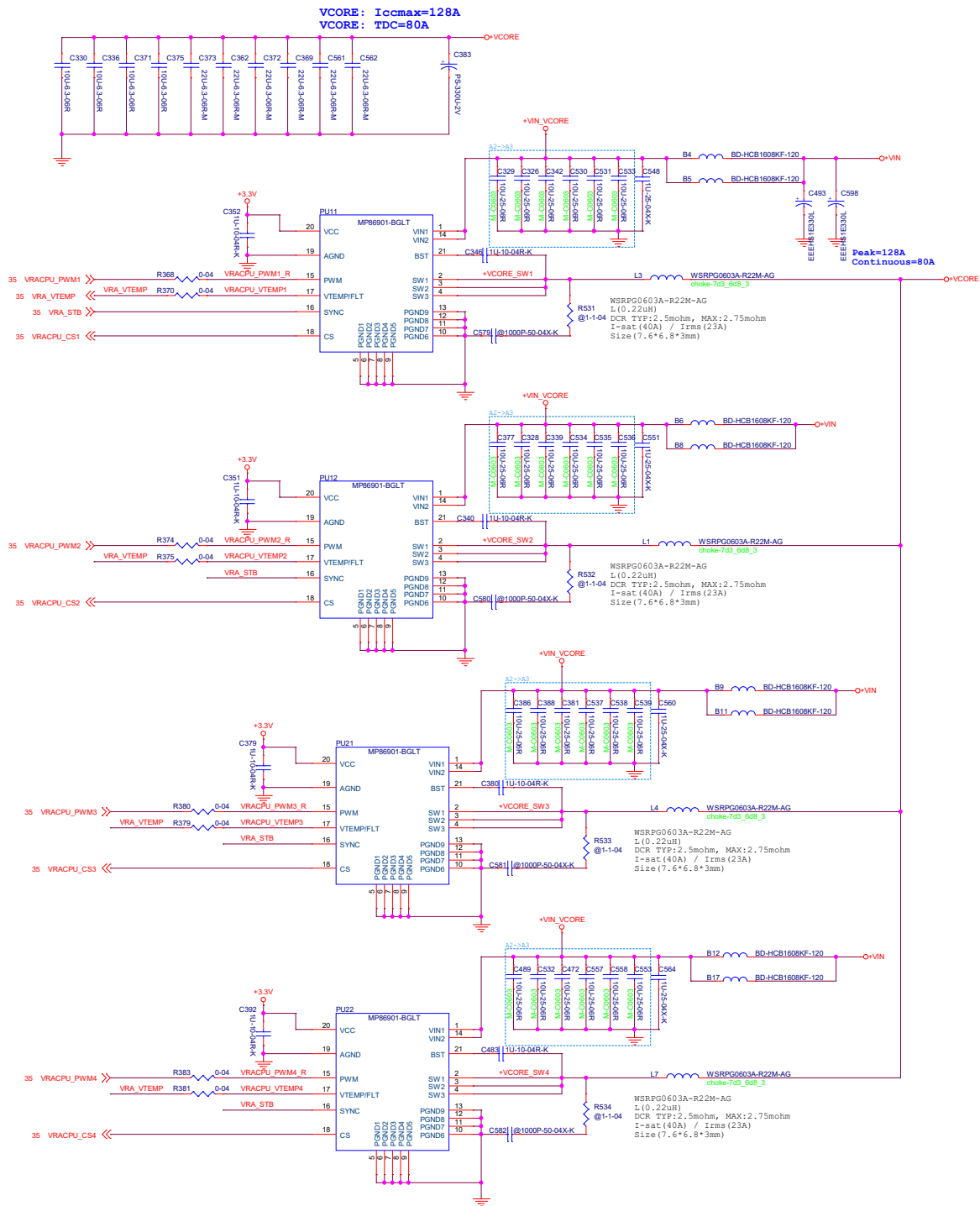


For RF

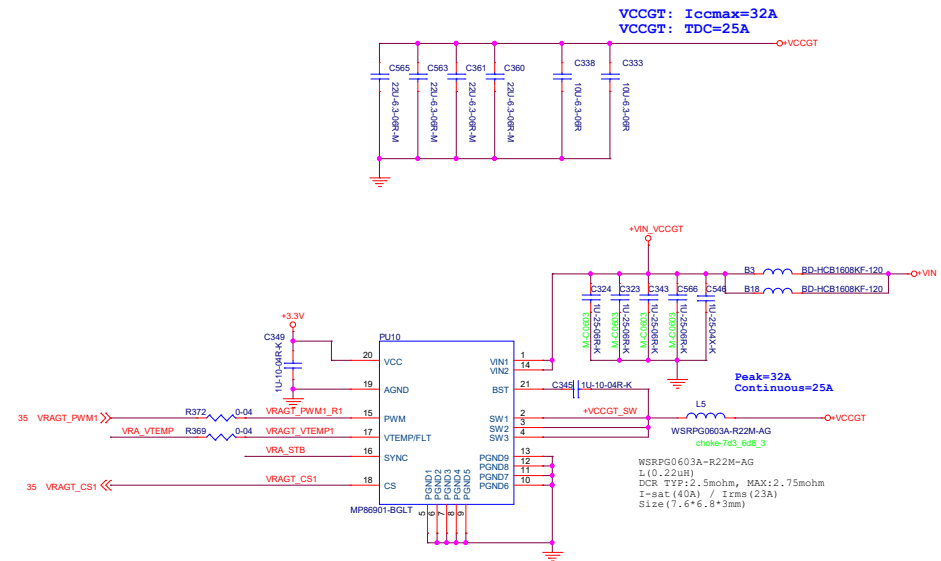




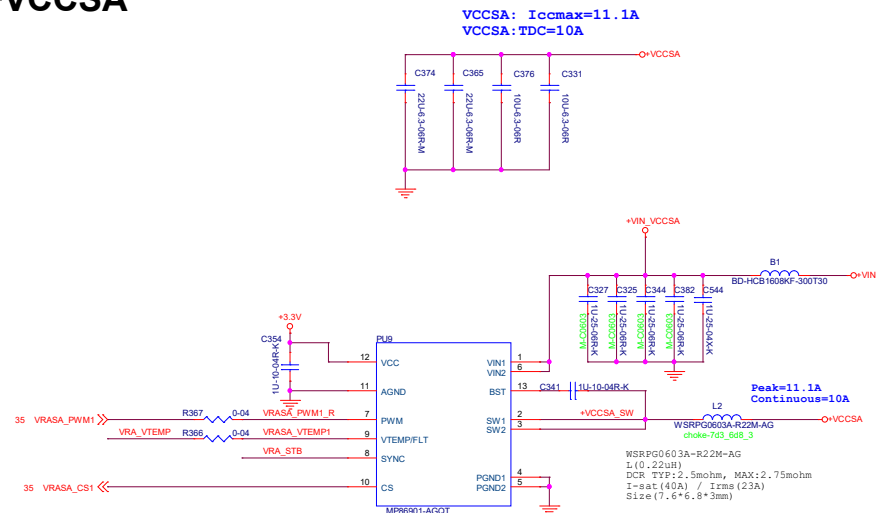
**+VCORE**



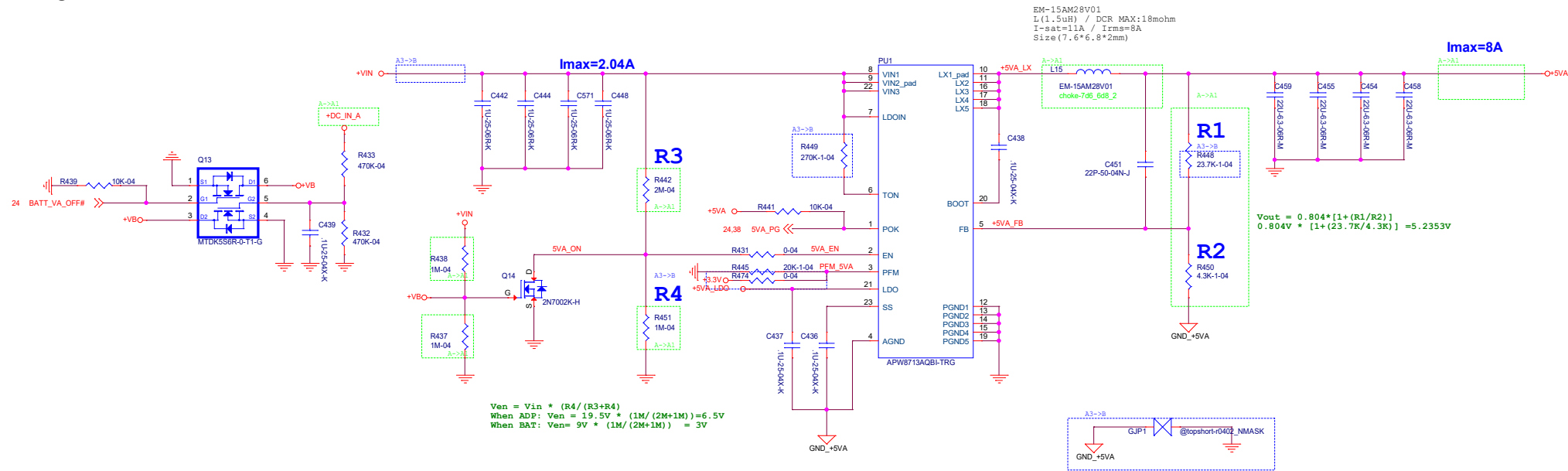
**+VCCGT**



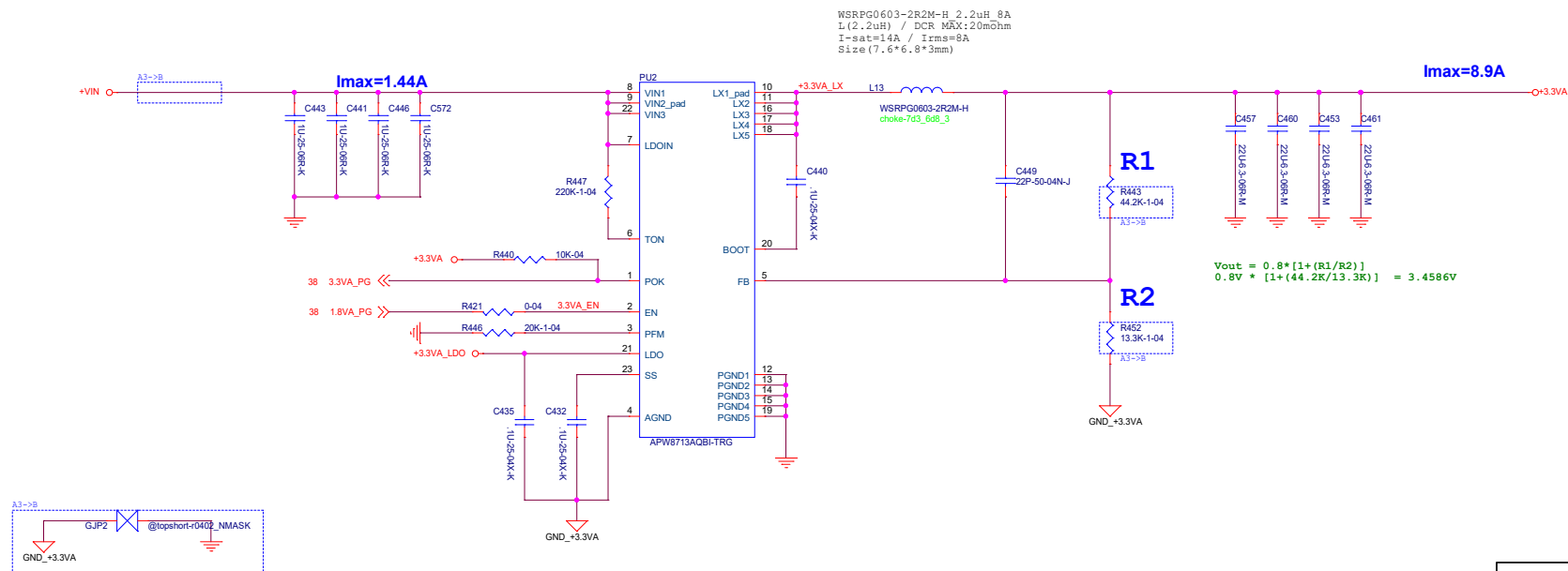
**+VCCSA**



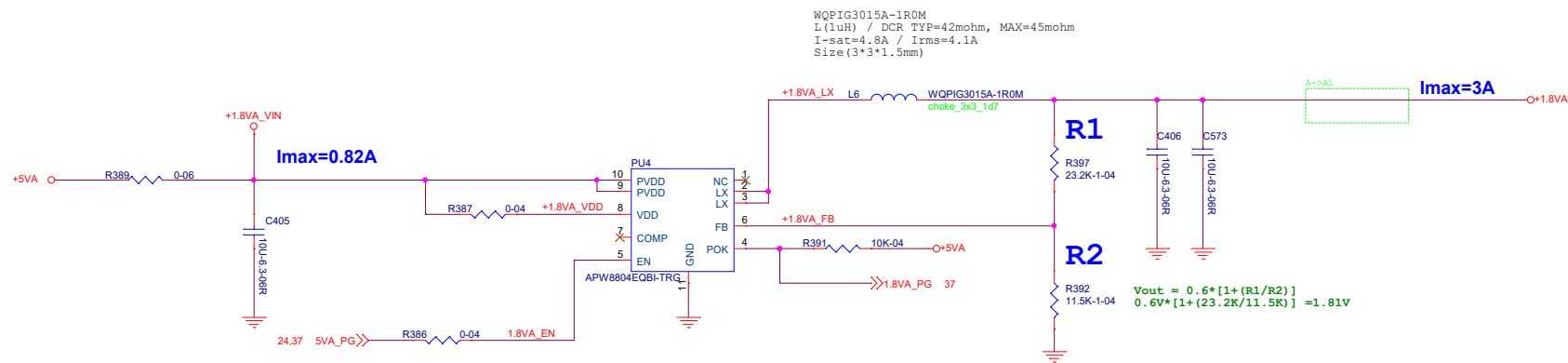
# +5VA



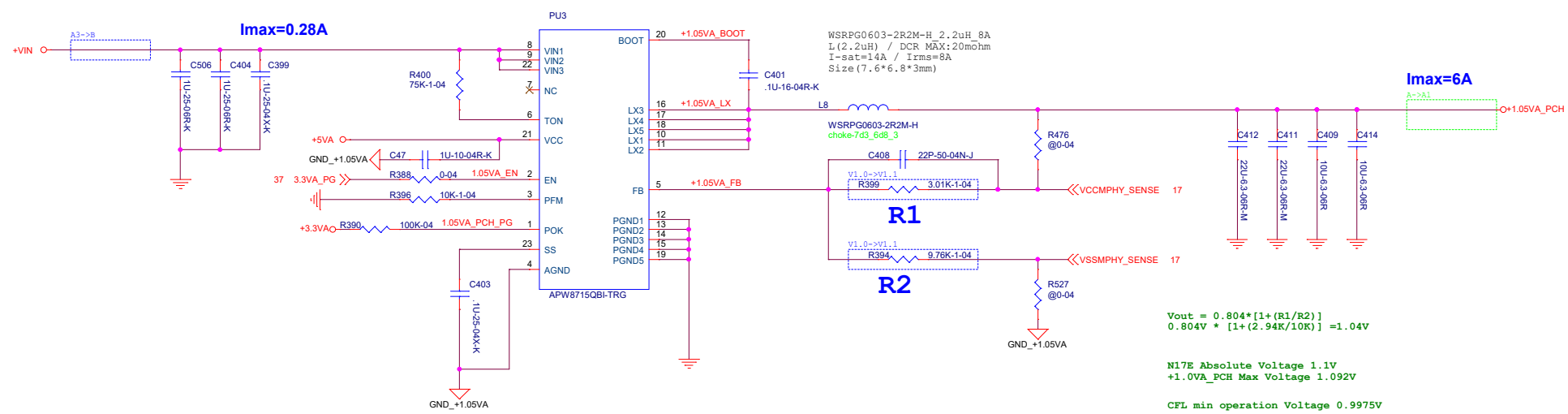
# +3.3VA



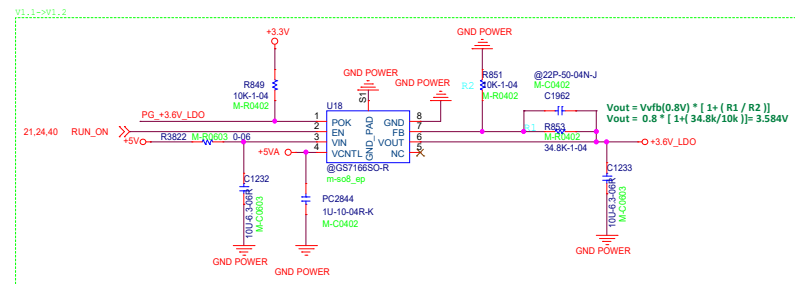
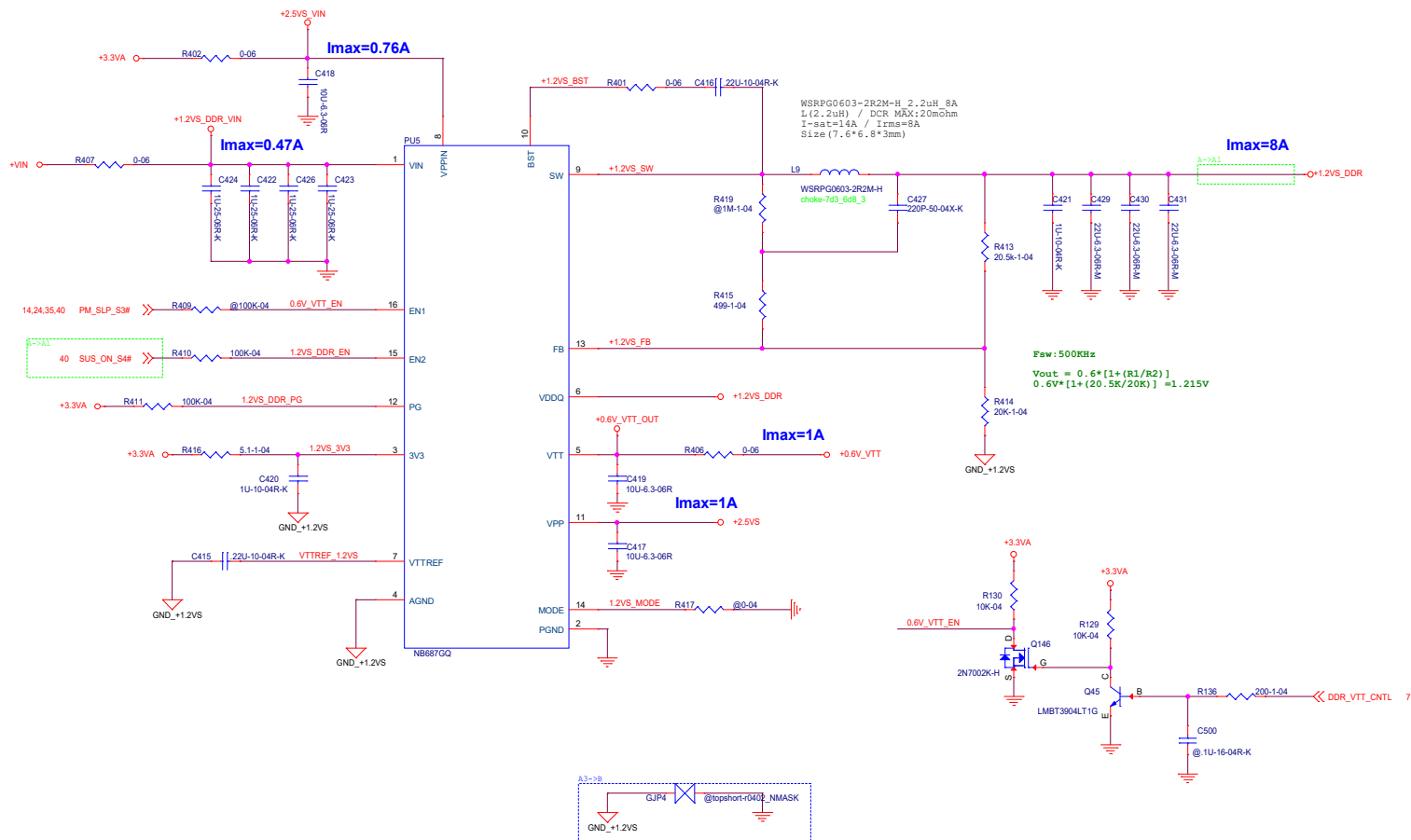
+1.8VA



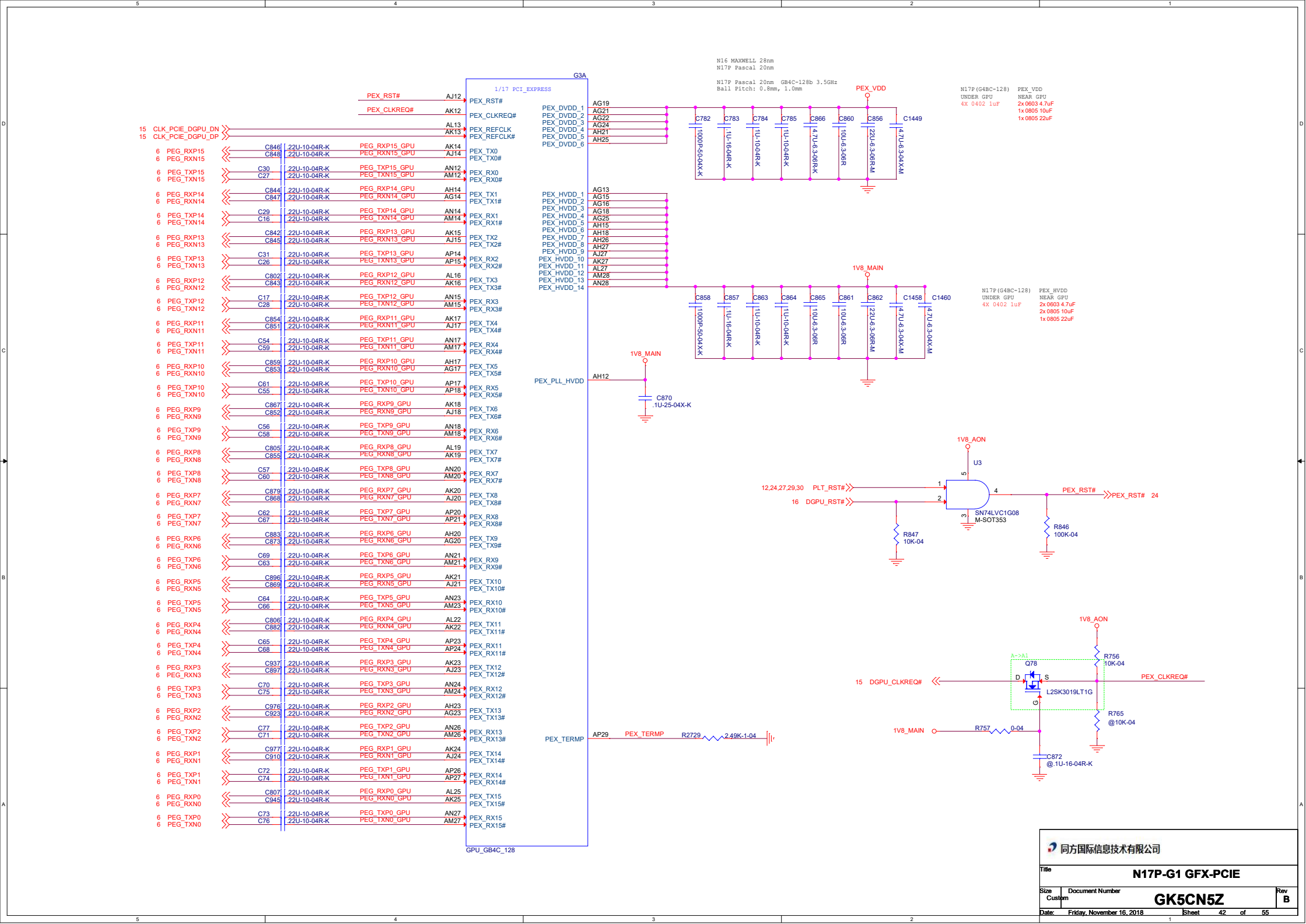
+1.05VA\_PCH



**+1.2VS\_DDR/+2.5VS/+0.6V\_VTT**

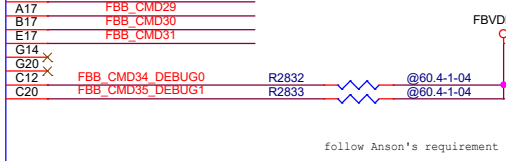
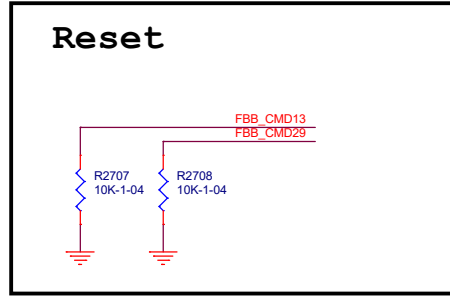
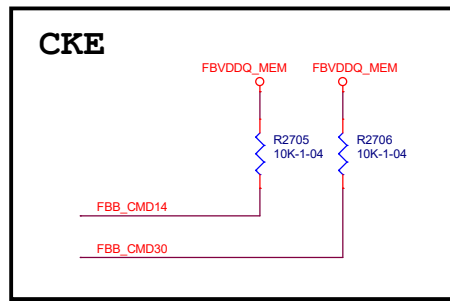
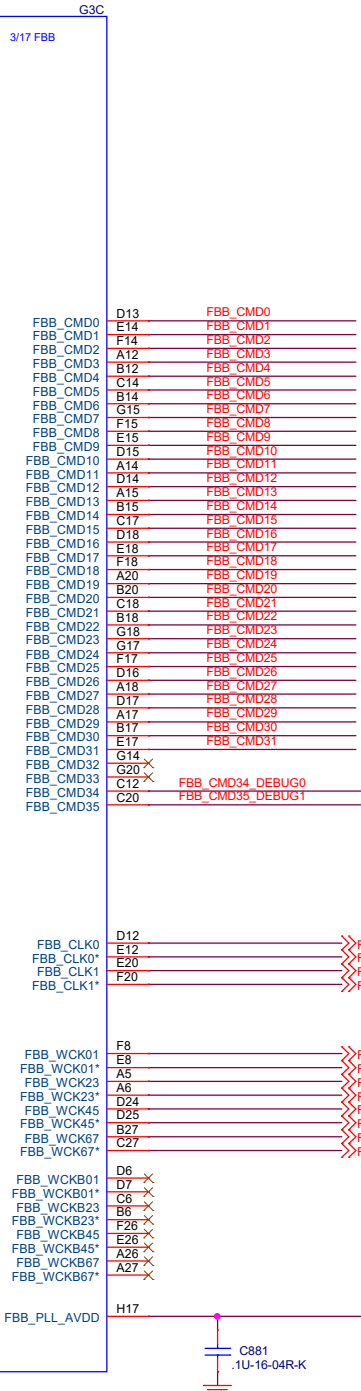
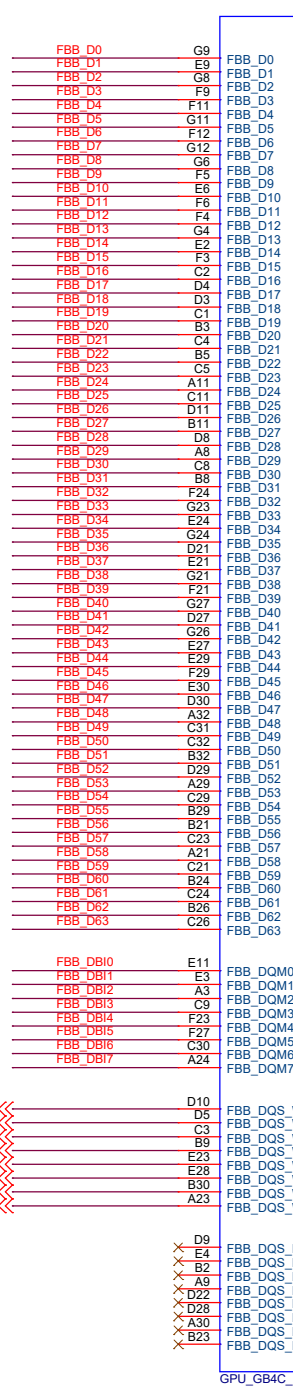
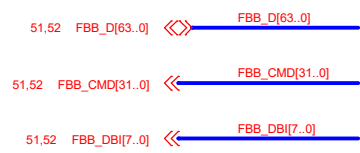


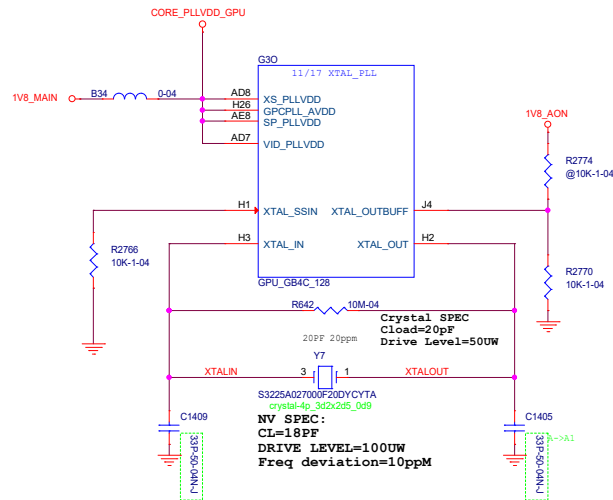
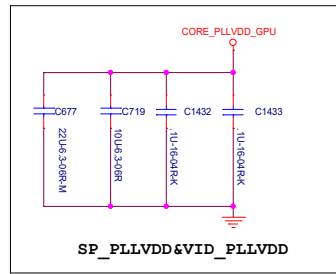
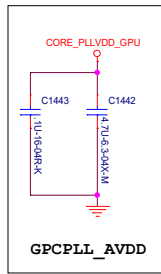
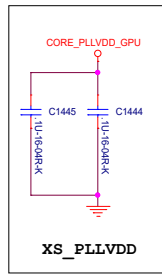












$$CL_{trim} = 2 * (C_{load} + (C_{stray} + C_i))$$

$$CL_{trim} = 2 * C_{load} - (3+5) =$$

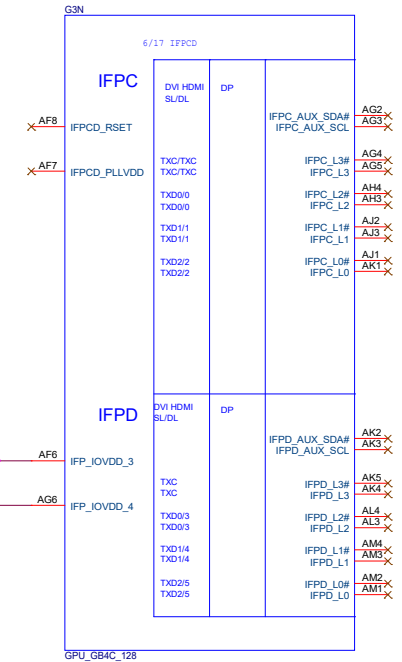
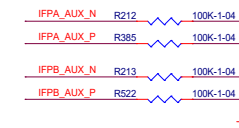
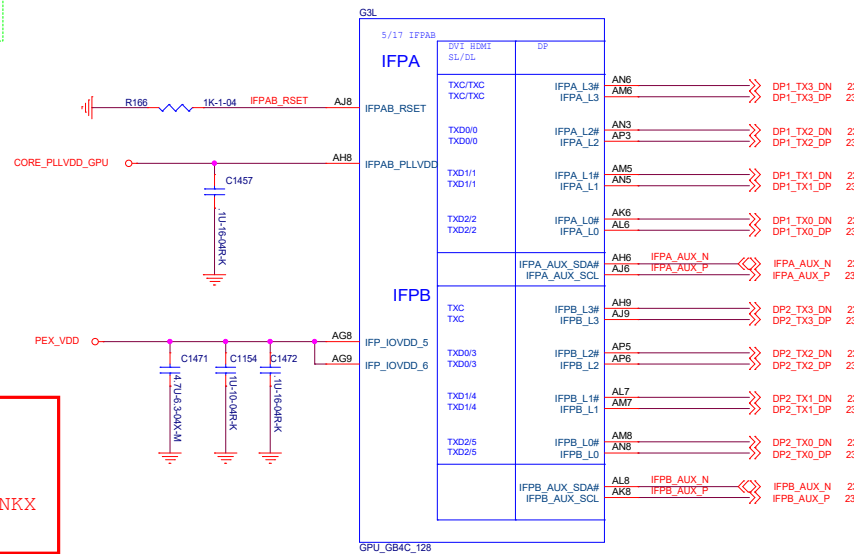
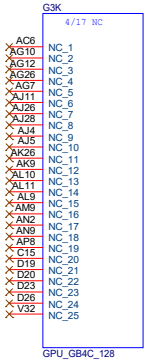
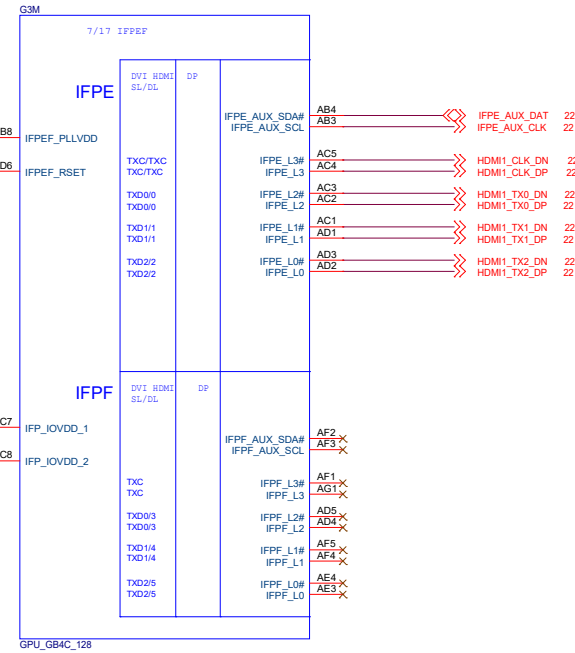
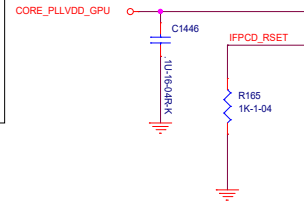
Where:

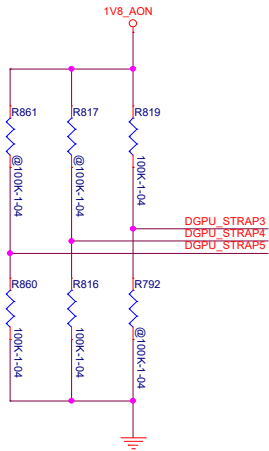
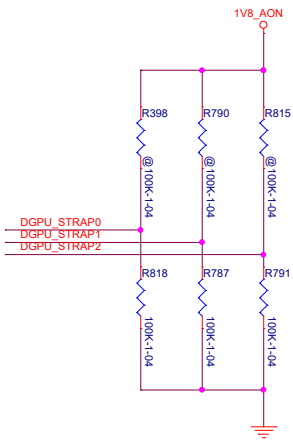
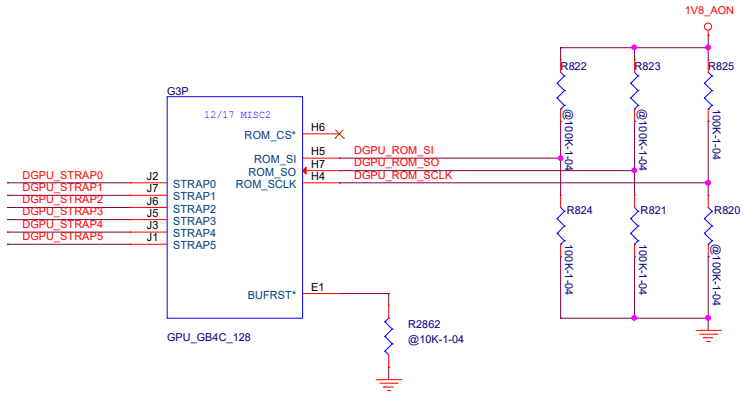
- ▶  $C_{load}$  is the crystal load capacitance (from data sheet of XTAL used)
- ▶  $C_{stray}$  is 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- ▶  $C_i$  is pin capacitance (5 pF)

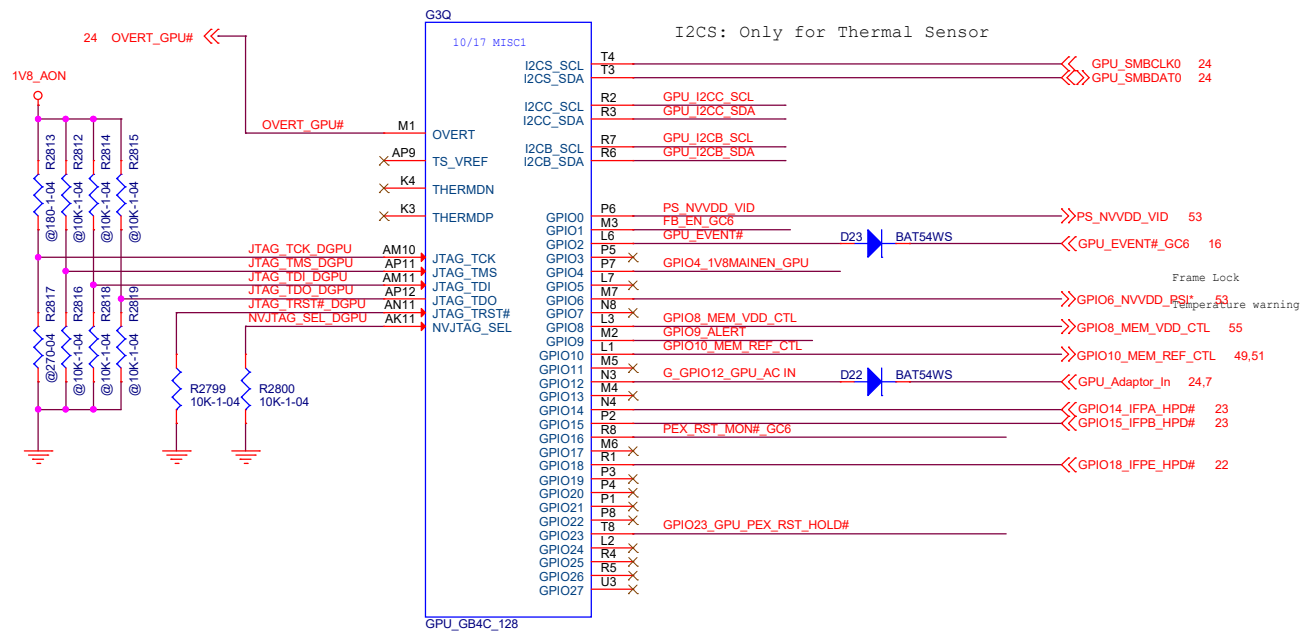
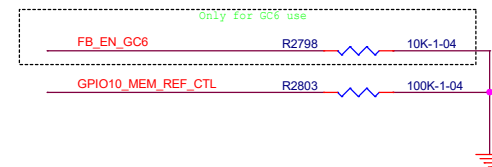
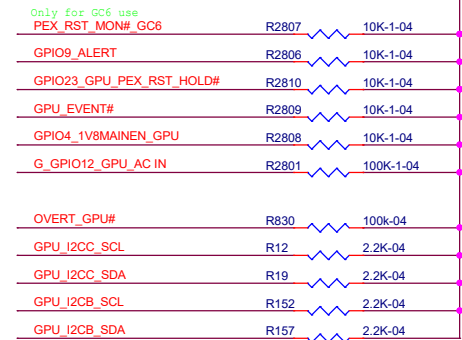
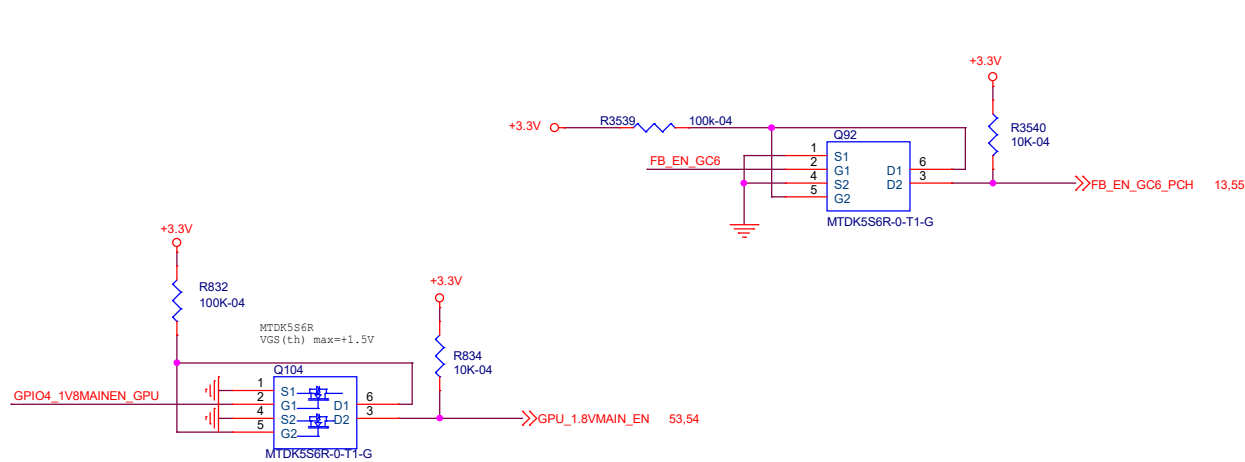
Typical CL trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

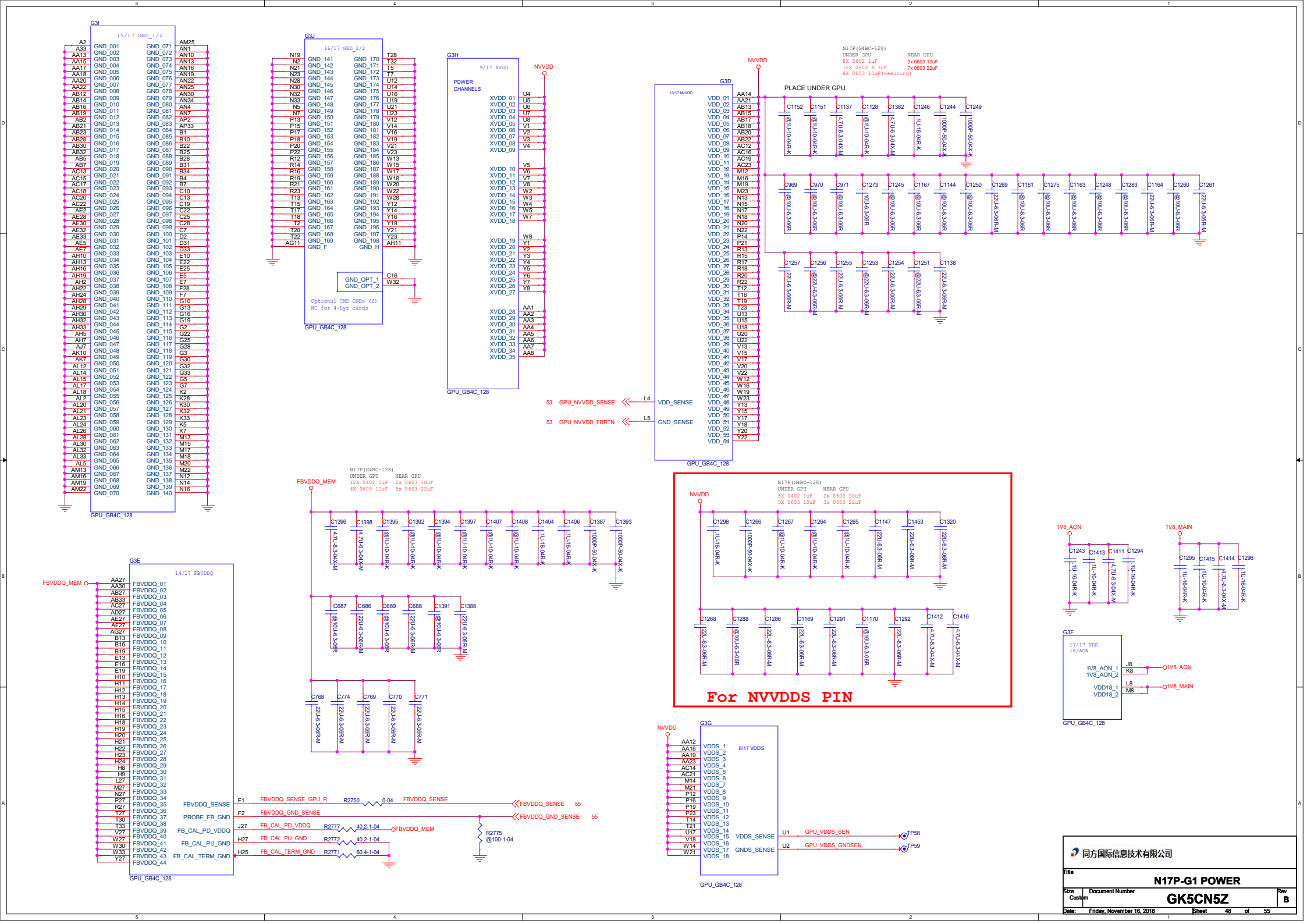
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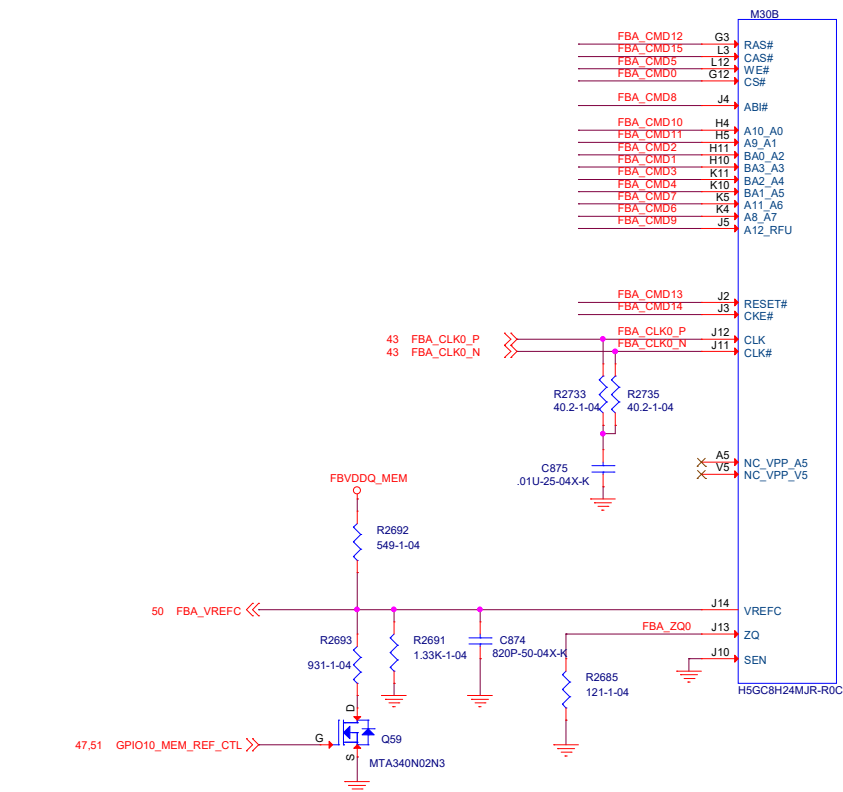
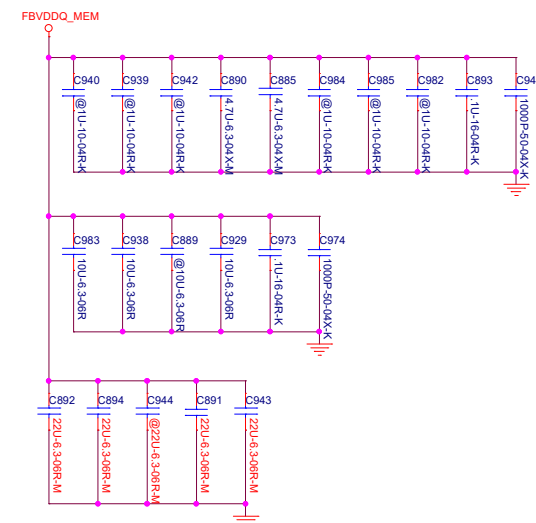
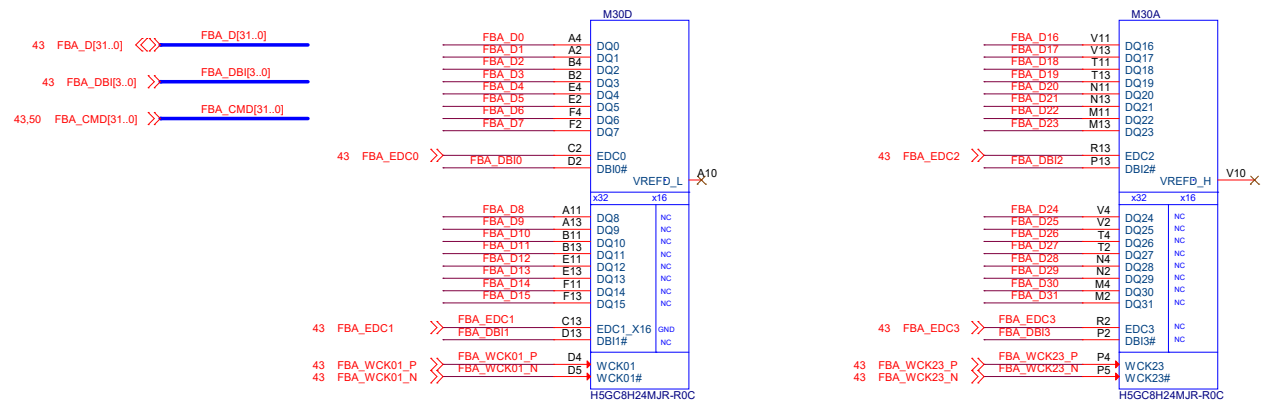
Hardware Design Guide Page282:  
 For IFPA/B/C/D/E/F  
 If an IFP link is not used,  
 it should be NC including power rail  
 and signal and references associated with LINKX







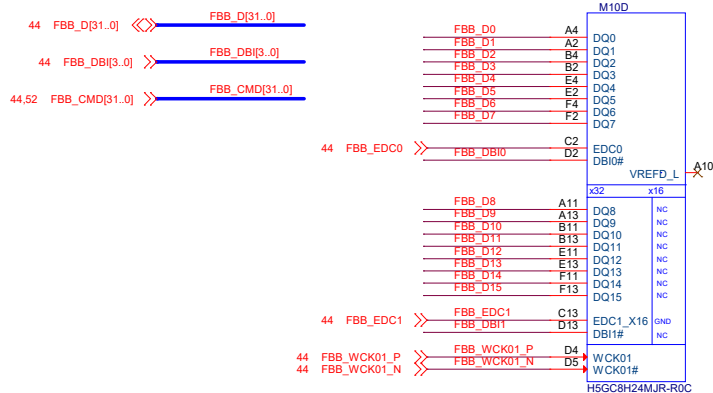




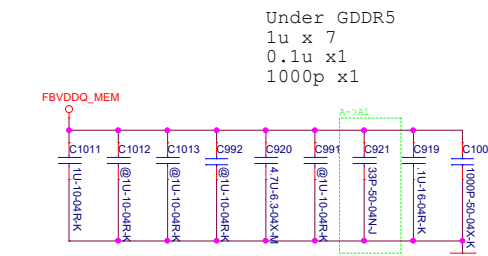
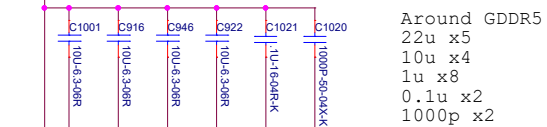
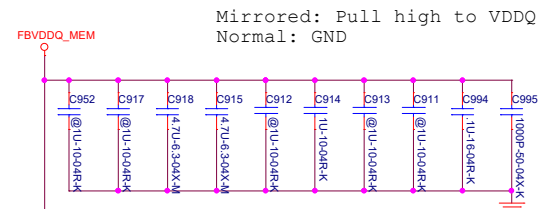
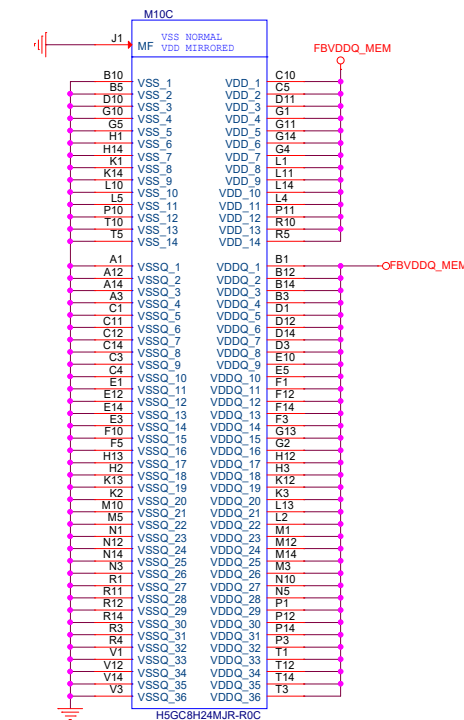
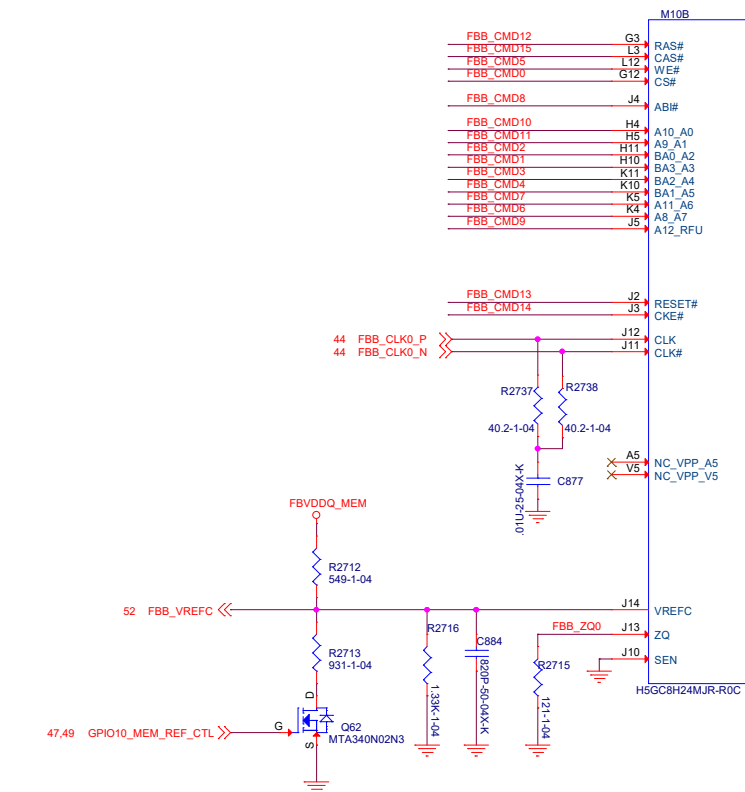




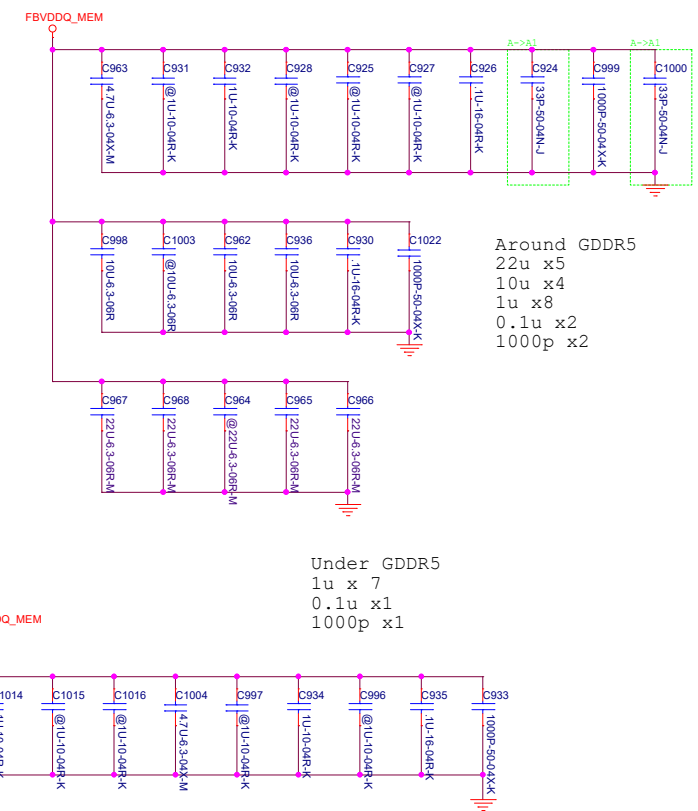
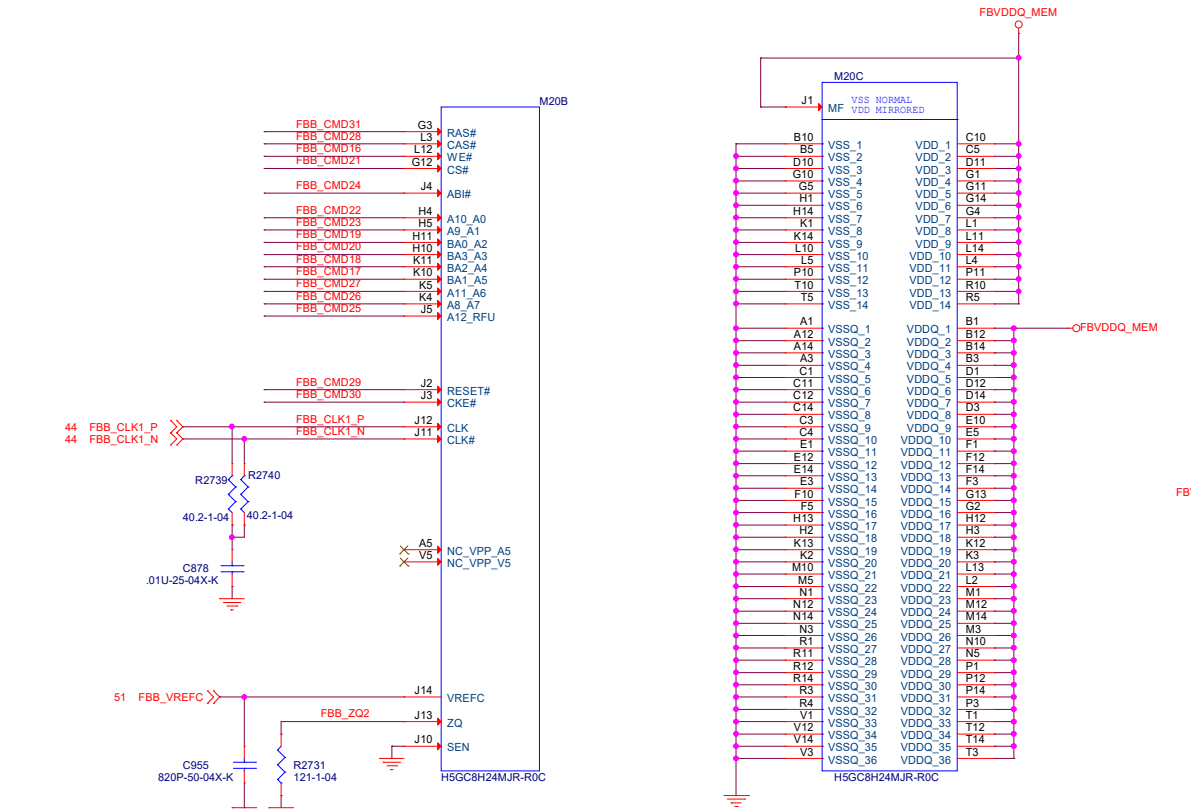
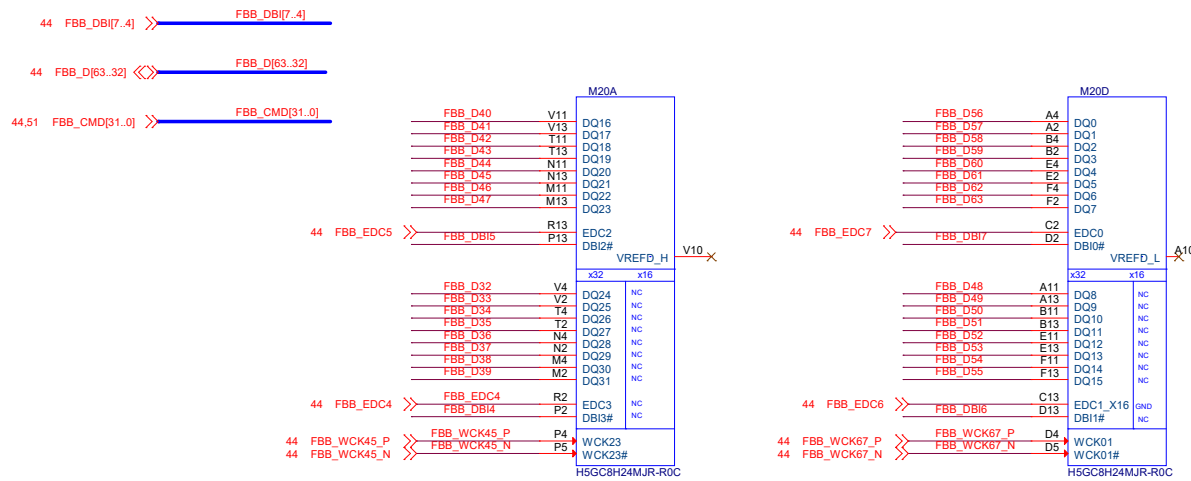




Maximum VRAM case Temp is 85 celcius degree



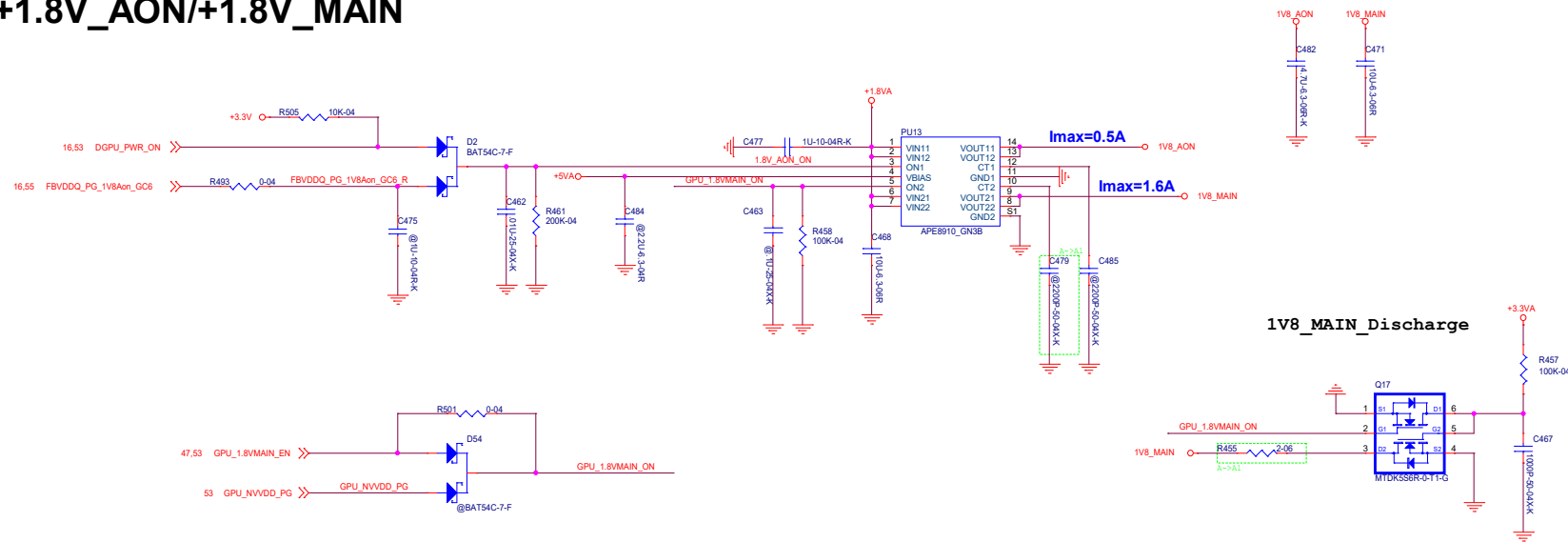
Maximum VRAM case Temp is 85 celcibus degree



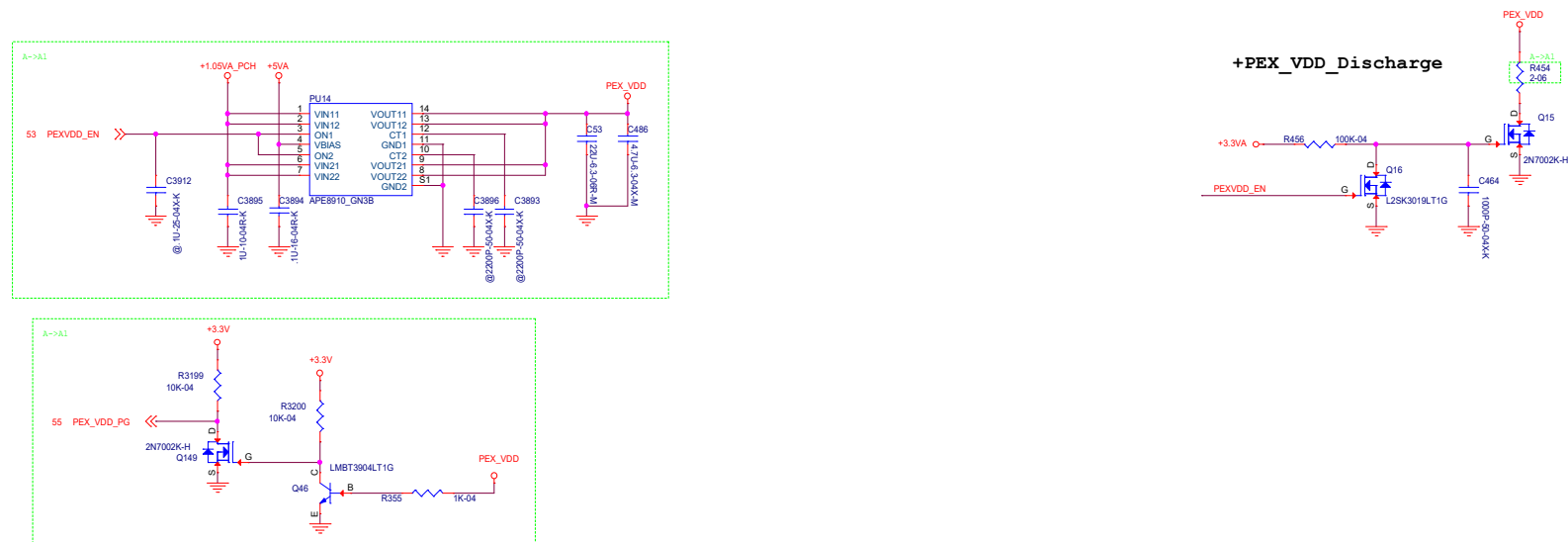
BOM option	
uP9509	UP1642T
R971=300K	R971=82K
R955=150ohm	R955=140ohm
C2552=1.000pF	C2552=4700pF
R950=30K	R950=40K
C2880=22K	C2880=40K
R979=1Kohm	R979=14..3Kohm
R984=2Kohm	R984=14..3Kohm
R985=51.0ohm	R985=14..3Kohm



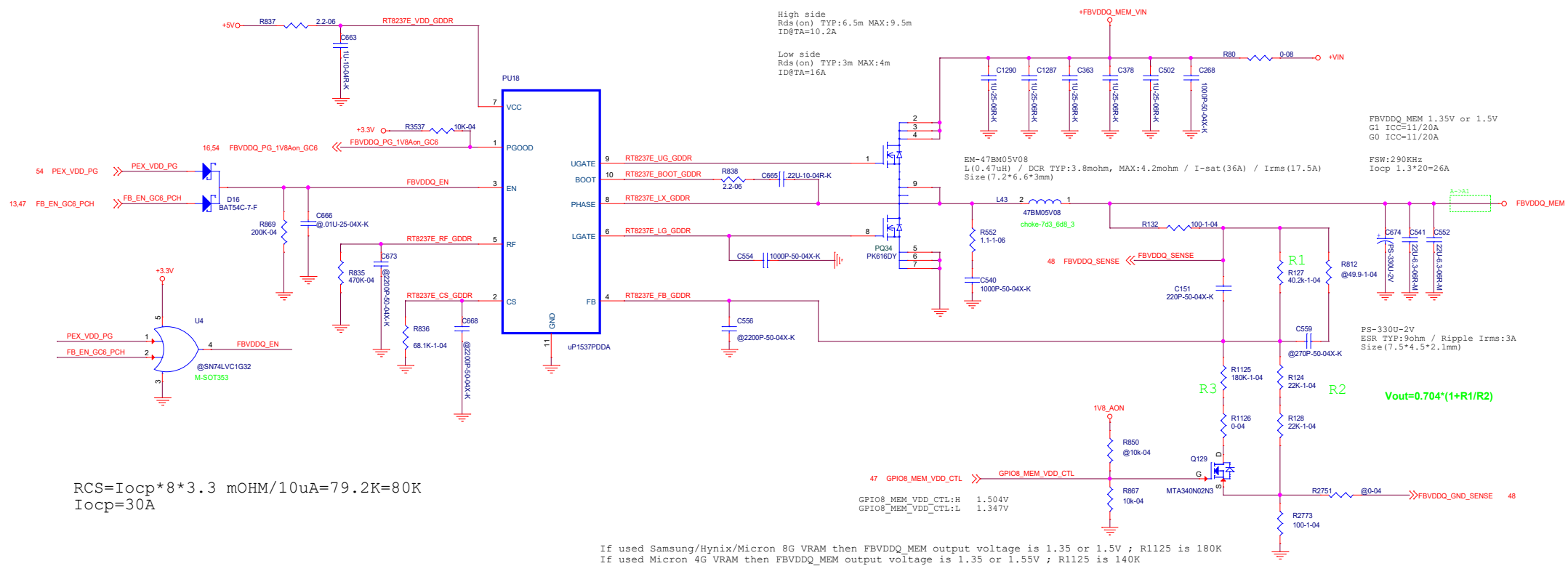
## +1.8V\_AON/+1.8V\_MAIN



**PEX\_VDD**



FBVDDQ\_MEM



FBVDDQ\_MEM\_Discharge

